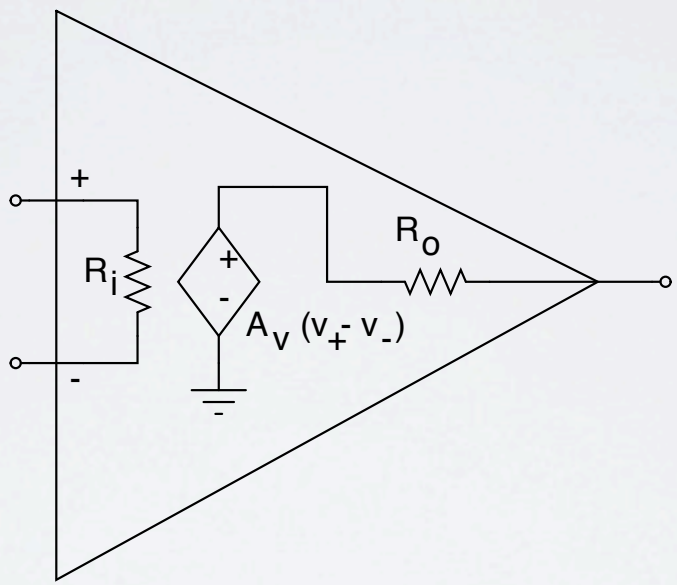
OFFSETS & BIAS

INEL 5207 - Spring 2013

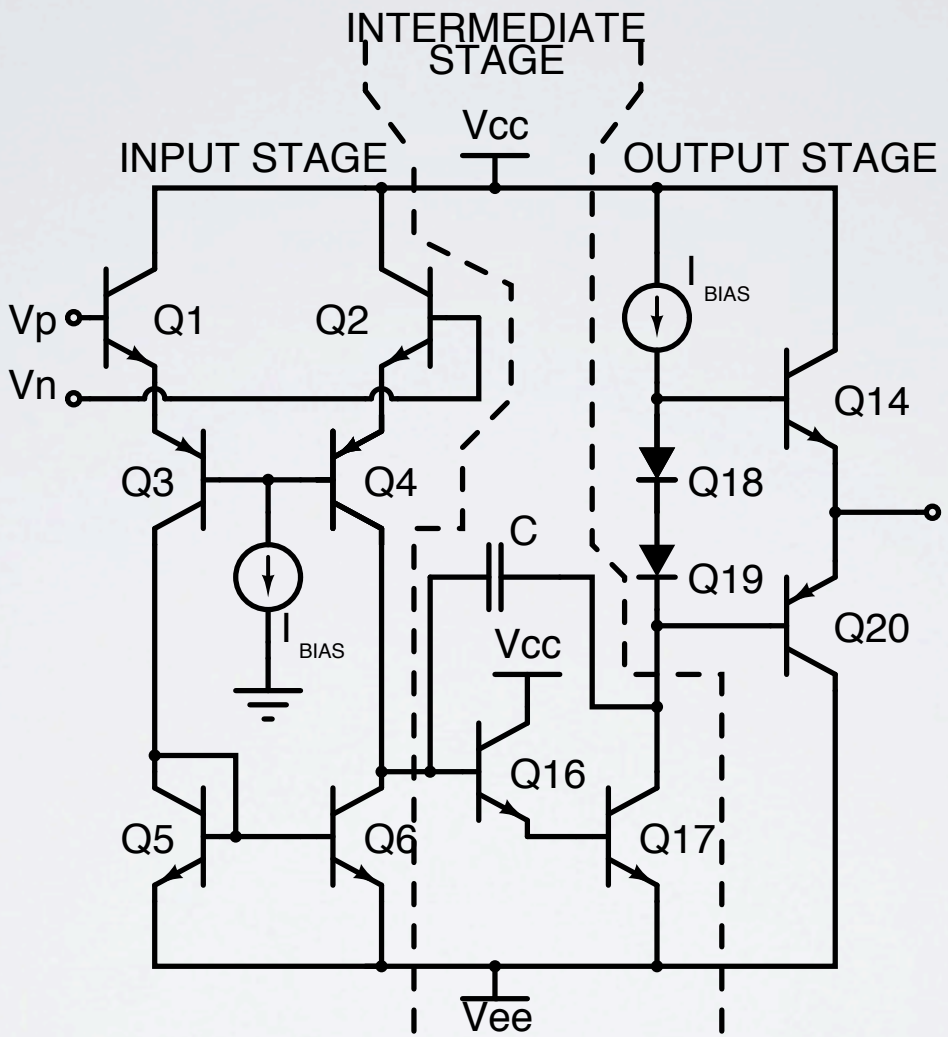
Operational Amplifier Limitations

Realistic Opamp Model: Finite gain, input and output resistance



Maximum Ratings

- Power supply voltages, power dissipation
- Common and differential-mode voltage range
- Short-circuit or overload output current protection
- First stage output is nonlinear for large differential input. $i_{o1} = I_A tanh \frac{v_p - v_n}{2V_T}$.
- Output voltage swing can reach saturation.



uA741 Simplified Schematic Diagram

Bias Current

- I_B: Bias current. Average current flowing into grounded inputs:

$$I_B = \frac{I_p + I_n}{2}$$

- I_{OS}: Offset current. Absolute value of the difference between input currents:

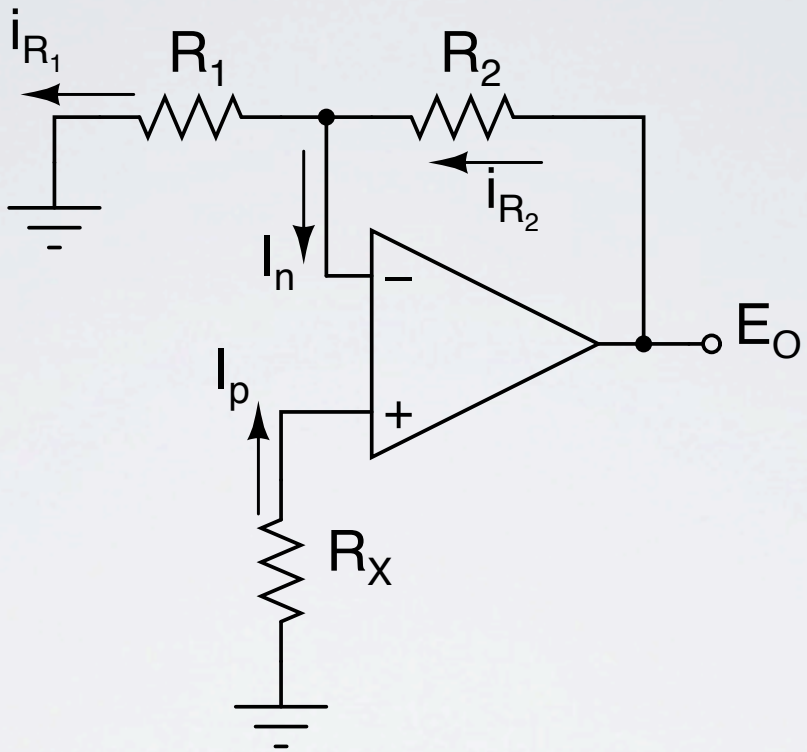
$$I_{OS} = \mid I_p - I_n \mid$$

- I_B flows into opamps with NPN-BJTs in the first stage, out for PNPs.

- Offset current sign can not be predicted and changes from device to device.

- The offset current is typically an order of magnitude smaller that the bias current.

- Error due to bias currents:



Assume input terminals are virtually connected.

$$v_n = v_p = -I_p R_x$$

and

$$I_{R_1} = -\frac{R_x}{R_1} I_p$$

Output error is then given by

$$E_O = -I_p R_x + \left(I_n - \frac{R_x}{R_1} I_p \right) R_2$$

Example: neglect I_{OS} and assume $I_p = I_n = 80\text{nA}$, for $R_x = 0$, $R_1 = 22k\Omega$, and $R_2 = 2.2M\Omega$

$$E_O = \left(2.2 \times 10^6\right)\left(80 \times 10^{-9}\right) = 0.176V$$

To reduce error:

- reduce size of R_2 and R_1

- select $R_x = R_1 \,||\, R_2$ to cancel the error due to I_B

We are left out with the error due to I_{OS}.

Bias Current Temperature Drift

- BJT: decrease with T because β increases with T
- JFET: doubles with every $10°C$ increase.

$$I_B(T) = I_B(T_0) \times 2^{(T-T_0)/10}$$

- MOSFET: similar to JFET due to presence of electrostatic-discharge protection diodes.

Low Input Bias Current Opamps

Part No.	Mfg	type	I_B	I_{OS}
741C		bjt	80nA	20nA
OP-77		bjt	1.2nA	0.3nA
LM308		superbeta	1nA	
OP-07		cancellation	1nA	0.4nA
LF356		biFET	30pA	3pA
AD549		biFET	below 100fA	
OPA129		biFET	below 100fA	
TLC279		CMOS	0.7pA	0.1pA

- Superbeta: use very thin base to produce very high β transistors.

- Input-bias-current cancellation: additional circutry provides the input transistor current internally. Looks like $I_B = 0$ from outside. I_{OS} and I_B are same order magnitute.

- biFET: use JFET front end, bipolar elsewhere.

- biMOS: use MOSFET front end, bipolar elsewhere.

- CMOS: use CMOSFETS only.

Input Offset Voltage, V_{OS}

- $v_{out} \neq 0$ when intput terminals are grounded

- Works like an offset in one input,

$$V_{OS} = \frac{v_{og}}{a}$$

  where v_{og} is v_o when inputs are grounded, a is open-loop gain.

- V_{OS} gain is same than signal.

- Both V_{OS} and I_B will cause integrators to saturate.

- Varies linearly with temperature. Typical temperature coefficient is $5mV/°C$ (741), $0.1mV/°C$ (OP-77).

- Changes with common-mode voltage:

$$\frac{dV_{OS}}{dv_{CM}} = \frac{1}{CMRR}$$

  Since CMRR drops with frequency, V_{OS} increases with f. Since $v_{CM} \approx v_p \approx v_n$, we can use v_p in the above formula.

- Changes with power supply voltage variations.

$$\frac{dV_{OS}}{dV_S} = \frac{1}{PSRR}$$

- Changes with output swing because $v_n - v_p$ change. $\Delta V_{OS} = \frac{\Delta v_{out}}{a}$.

EFFECT OF COMMON-MODE SIGNALS & CMRR

$$v_O = av_d + \frac{a}{CMRR}v_{CM} \rightarrow \frac{\partial v_O}{\partial v_{CM}} = \frac{a}{CMRR}$$

The effect of the CM signal can be expressed as a change in the input offset

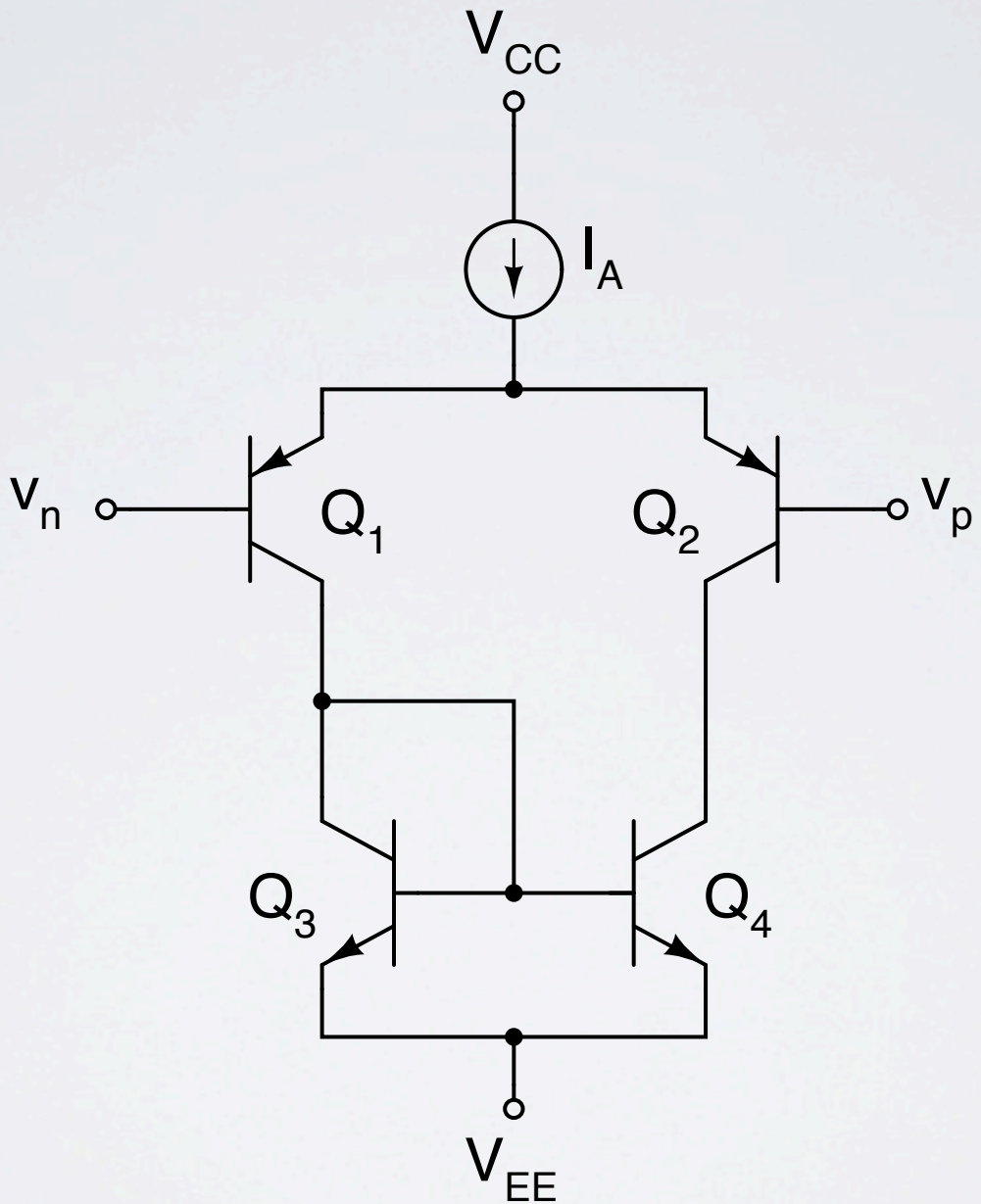
$$\frac{\partial V_{OS}}{\partial v_{CM}} = \frac{1}{a}\frac{a}{CMRR} = \frac{1}{CMRR}$$

$$\Delta V_{OS} = \frac{\Delta v_{CM}}{CMRR} \approx \frac{\Delta v_P}{CMRR}$$

If application uses an inverting configuration, $v_P = 0$ and v_{CM} has no effect.

- Summarizing,

$$V_{OS} = V_{OS0} + TC \times \Delta T + \frac{\Delta v_p}{CMRR} + \frac{\Delta V_s}{PMRR} + \frac{\Delta v_{out}}{a}$$


V_{CC}
I_A
v_n
Q_1
Q_2
v_p
Q_3
Q_4
V_{EE}

Techniques to reduce V_{OS}

- For BJT opamps

$$V_{OS} = V_T ln \frac{I_{s1}}{I_{s2}} \frac{I_{s4}}{I_{s3}}$$

- A 10% mismatch in I_s's give $V_{OS} = 2.4mV$ at 300K.

- Since $V_T = \frac{kT}{q}$,

$$TC_{V_{OS}} = \frac{V_{OS}}{T}$$

- I_s also depend on temperature:

$$I_s = \frac{qD_n}{N_B} \times n_i^2(T) \times \frac{A_E}{W_B}$$

- Fabrication process variations affect A_E, W_B, N_B. Large device size helps reduce these errors.

- Improved layout (*common-centroid layout*) can reduce thermal gradients and thus the effect of temperature.

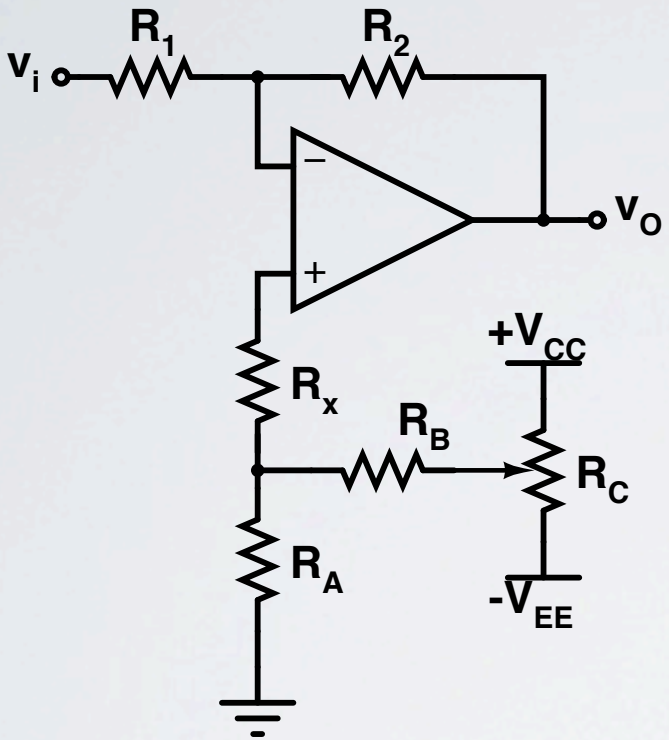
- On-chip laser (known as *Zener zapping*) trimmings can be added to the circuit to reduce V_{OS}.

- *Chopper-stabilized*, or *autozero opamps* include internal circutry to periodicaly correct V_{OS} and keep it at a minimum.

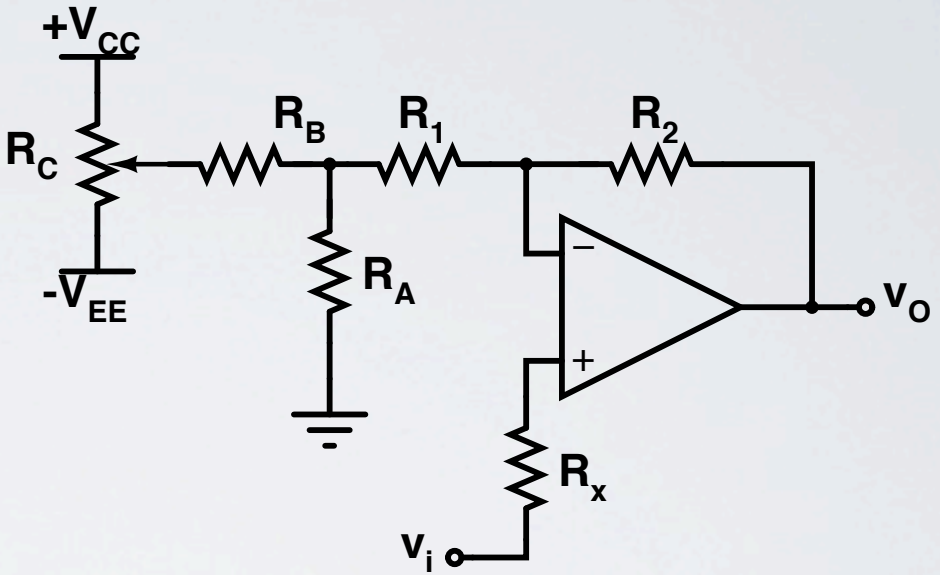
Offset Nulling

- Many opamps have terminals for offset nulling.

- External trimming can also be used to correct for V_{OS} and I_{OS}.



inverting



non-inverting

Offset Nulling Networks