Operational Amplifier Limitations

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1 Realistic Opamp Model

Finite gain, input and output resistance

\[ A(v_+ - v_-) \]

\[ R_i \]

\[ R_o \]

2 Maximum Ratings

- Power supply voltages, power dissipation
- Common and differential-mode voltage range
- Short-circuit or overload output current protection
- First stage output is nonlinear for large differential input. \( i_{o1} = I_A tanh \frac{v_n - v_m}{2V_T} \).
- Output voltage swing can reach saturation.
3 Bias Current

- $I_B$: Bias current. Average current flowing into grounded inputs:

$$I_B = \frac{I_p + I_n}{2}$$

- $I_{OS}$: Offset current. Absolute value of the difference between input currents:

$$I_{OS} = |I_p - I_n|$$

- $I_B$ flows into opamps with NPN-BJT$\bar{s}$ in the first stage, out for PNPs.
- Offset current sign can not be predicted and changes from device to device.
- The offset current is typically an order of magnitude smaller that the bias current.
3.1 Error due to bias currents

Assume input terminals are virtually connected.

\[ v_n = v_p = -I_p R_x \]

and

\[ I_{R_1} = -\frac{R_x}{R_1} I_p \]

Output error is then given by

\[ E_O = -I_p R_x + \left( I_n - \frac{R_x}{R_1} I_p \right) R_2 \]

Example: neglect \( I_{OS} \) and assume \( I_p = I_n = 80 \text{nA} \), for \( R_x = 0 \), \( R_1 = 22 \text{k} \Omega \), and \( R_2 = 2.2 \text{M} \Omega \)

\[ E_O = \left( 2.2 \times 10^6 \right) \left( 80 \times 10^{-9} \right) = 0.176V \]

To reduce error:

- reduce size of \( R_2 \) and \( R_1 \)
- select \( R_x = R_1 \parallel R_2 \) to cancel the error due to \( I_B \)

We are left out with the error due to \( I_{OS} \).

3.2 Bias Current Temperature Drift

- BJT: decrease with \( T \) because \( \beta \) increases with \( T \)
- JFET: doubles with every \( 10^\circ C \) increase.

\[ I_B(T) = I_B(T_0) \times 2^{(T-T_0)/10} \]

- MOSFET: similar to JFET due to presence of electrostatic-discharge protection diodes.
3.3 Low Input Bias Current Opamps

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Mfg</th>
<th>type</th>
<th>$I_B$</th>
<th>$I_{OS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>741C</td>
<td>bjt</td>
<td>80nA</td>
<td>20nA</td>
<td></td>
</tr>
<tr>
<td>OP-77</td>
<td>bjt</td>
<td>1.2nA</td>
<td>0.3nA</td>
<td></td>
</tr>
<tr>
<td>LM308</td>
<td>superbeta</td>
<td>1nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OP-07</td>
<td>cancellation</td>
<td>1nA</td>
<td>0.4nA</td>
<td></td>
</tr>
<tr>
<td>LF356</td>
<td>biFET</td>
<td>30pA</td>
<td>3pA</td>
<td></td>
</tr>
<tr>
<td>AD549</td>
<td>biFET</td>
<td>below 100fA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA129</td>
<td>biFET</td>
<td>below 100fA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TLC279</td>
<td>CMOS</td>
<td>0.7pA</td>
<td>0.1pA</td>
<td></td>
</tr>
</tbody>
</table>

- Superbeta: use very thin base to produce very high $\beta$ transistors.
- Input-bias-current cancellation: additional circuitry provides the input transistor current internally. Looks like $I_B = 0$ from outside. $I_{OS}$ and $I_B$ are same order magnitude.
- biFET: use JFET front end, bipolar elsewhere.
- biMOS: use MOSFET front end, bipolar elsewhere.
- CMOS: use CMOSFETS only.

4 Input Offset Voltage, $V_{OS}$

- $v_{out} \neq 0$ when input terminals are grounded
- Works like an offset in one input, $V_{OS} = \frac{v_{og}}{a}$
  
  where $v_{og}$ is $v_o$ when inputs are grounded, $a$ is open-loop gain.
- $V_{OS}$ gain is same than signal.
- Both $V_{OS}$ and $I_B$ will cause integrators to saturate.
- Varies linearly with temperature. Typical temperature coefficient is $5mV/^\circ C$ (741), $0.1mV/^\circ C$ (OP-77).
- Changes with common-mode voltage:
  
  \[
  \frac{dV_{OS}}{dv_{CM}} = \frac{1}{CMRR}
  \]

  Since CMRR drops with frequency, $V_{OS}$ increases with $f$. Since $v_{CM} \approx v_p \approx v_n$, we can use $v_p$ in the above formula.
• Changes with power supply voltage variations.

\[
\frac{dV_{OS}}{dV_s} = \frac{1}{P SRR}
\]

• Changes with output swing because \(v_n - v_p\) change. \(\Delta V_{OS} = \frac{\Delta v_{out}}{a}\).

• Summarizing,

\[
V_{OS} = V_{OS0} + TC \times \Delta T + \frac{\Delta v_p}{CMRR} + \frac{\Delta V_s}{PMRR} + \frac{\Delta v_{out}}{a}
\]

### 4.1 Techniques to reduce \(V_{OS}\)

![Bipolar transistor schematic](image)

• For BJT opamps

\[
V_{OS} = V_T \ln \frac{I_{s1} I_{s4}}{I_{s2} I_{s3}}
\]

• A 10% mismatch in \(I_s\)'s give \(V_{OS} = 2.4mV\) at \(300K\).

• Since \(V_T = \frac{kT}{q}\),

\[
TCV_{OS} = \frac{V_{OS}}{T}
\]

• \(I_s\) also depend on temperature:

\[
I_s = \frac{qD_n}{N_B} \times n_i^2(T) \times \frac{A_E}{W_B}
\]

• Fabrication process variations affect \(A_E, W_B, N_B\). Large device size helps reduce these errors.

• Improved layout (common-centroid layout) can reduce thermal gradients and thus the effect of temperature.

• On-chip laser (known as Zener zapping) trimmings can be added to the circuit to reduce \(V_{OS}\).

• Chopper-stabilized, or autozero opamps include internal circuitry to periodically correct \(V_{OS}\) and keep it at a minimum.
4.2 Offset Nulling

- Many opamps have terminals for offset nulling.
- External trimming can also be used to correct for $V_{OS}$ and $I_{OS}$.

![Offset Nulling Networks](image)

5 Frequency Limits

- Many opamps are internally compensated to have a single dominant pole at a relatively low frequency.

![Frequency Limits](image)

5.1 Noninverting Amplifier

- Open-loop gain can be written as:

$$a(s) = a_0 \frac{1}{1 + s/\omega_p}$$

$$a_0 = \text{d.c. open-loop gain}; \quad f_p = \frac{1}{2\pi R_{eq}C_{eq}} = \text{pole freq.}$$
For the non-inverting amplifier

\[ A = \frac{a}{1 + a\beta} \]

where \( \beta = \frac{R_2}{R_1 + R_2} \).

Using above \( a(s) \) and \( A_0 = \frac{a_0}{1 + \beta a_0} \),

\[ A(s) = \frac{a(s)}{1 + a(s)\beta} = A_0 \frac{\omega_p(1 + \beta a_0)}{s + \omega_p(1 + \beta a_0)} \]

- Corner frequency is increased by \( 1 + \beta a_0 \). Gain is decreased by the same factor.
- Gain-bandwidth product remains constant and equal to unity gain frequency, \( f_t \).

\[ GBP = f_t \]

This is only true for \( \beta \) constant and compensated opamp (dominant pole at low freq.)

Gain of \( n \) identical noninverting stages

- If \( f_{cl} = \frac{\omega_p(1 + \beta a_0)}{2\pi} \), then gain magnitude of one stage is

\[ A = A_0 \frac{1}{\sqrt{1 + (f/f_{cl})^2}} \]

- Gain of \( n \) identical stages is

\[ A^n = A_0^n (1 + (f/f_{cl})^2)^{-n/2} \]

- At corner frequency \( f_{3dB} \), \( A^n/A_0^n = 1/\sqrt{2} \) (i.e. -3dB). Thus,

\[ f_{3dB} = f_{cl} \sqrt{2^{1/n} - 1} = \frac{f_t}{A_0} \sqrt{2^{1/n} - 1} \]

- To design an amplifier with bandwidth \( f_{bw} \) and gain \( K \), we must select \( n \) such that \( K = A_0^n \) and \( f_{bw} \leq \frac{f_t}{A_0} \sqrt{\frac{1}{2^n} - 1} \).

### 5.2 Inverting Amplifier

For the inverting amplifier, the gain-bandwidth product is equal to

\[ GBP = f_t \frac{R_2}{R_1 + R_2} \]

so the bandwidth is always lower than that of a non-inverting amplifier with the same gain.

- Equivalently, we can say that \( f_{bw} \times (1 + \frac{R_2}{R_1}) \) is still constant and equal to \( f_t \), but the amplifier’s gain magnitude of is only \( \frac{R_2}{R_1} \).
6 Input Impedance

- Diff. input impedance $r_d$ is typ. few $M\Omega$, common-mode $r_c$ is in the $G\Omega$ for BJT. FETs are in the 100’s $G\Omega$.
- Input capacitance for uA741 is about 1 pF. Appears in parallel with $r_d$ and/or $r_c$.
- For $f = 100kHz$, $X_c = 10M\Omega$ so it is comparable to $r_d$. At higher frequencies, input impedance drops due to the input capacitance.

$$z_d = \frac{r_d}{1 + sC_d r_d}$$

- There is also a common-mode impedance.

6.1 $Z_{in}$ for Input-series Feedback

![Diagram](image)

- $z_{df} = z_d(1 + a\beta)$. Using $a = \frac{a_0}{1+j\frac{f}{f_a}}$ yields

$$z_{df} = z_d(1 + a_0\beta) \frac{1 + j\frac{f}{f_a}}{1 + j\frac{f}{f_a}}$$

- Observe that $f_a$ is the open-loop pole. Since $a_0 f_a = GBP = f_t$, we can write $f_a = \frac{f_t}{a_0}$. Generally $1 + \beta a_0 \approx \beta a_0$; thus

$$f_a(1 + \beta a_0) \approx \beta a_0 f_a = \beta f_t$$

The above expression becomes

$$z_{df} = z_d(1 + a_0\beta) \frac{1 + j\frac{f}{f_a}}{1 + j\frac{f}{f_a}}$$
6.2 $Z_{in}$ for Input-shunt Feedback

$$Z_{in} = R_1 \frac{1}{1 + a\beta} = R_1 \frac{1 + j\frac{f}{f_c}}{1 + j\frac{f}{f_c}}$$

6.3 $Z_o$ for Output-series feedback

- $Z_{of} = R(1 + a\beta)$. Using $\beta = 1$ and our previous result

$$R_{of} = R(1 + a\beta) \frac{1 + j\frac{f}{f_c}}{1 + j\frac{f}{f_c}}$$

6.4 $Z_o$ for Output-shunt feedback

$$Z_o = \frac{r_o}{1 + \beta a} = r_o (1 + a\beta) \frac{1 + j\frac{f}{f_c}}{1 + j\frac{f}{f_c}}$$
7 Transient Response

• A follower have a gain given by \( A = \frac{1}{1+jf_0} \).

• Step response is \( v_o = V_m(1 - e^{-t/\tau}) \), where \( \tau = \frac{1}{2\pi f_t} \).

• Rise time \( t_r \) is time from 10% to 90% of \( V_m \).
  \[ t_r = \frac{0.35}{f_t} \]

• Ringing due to higher frequency poles.

7.1 Slew Rate

\[ i_{O1} \] is limited to \( \pm I_A \). Output can not change faster than

\[ SR = \frac{I_A}{C_C} \]

• Fastest part of step response occurs at \( t = 0 \), and is

\[ \frac{dv_O}{dt} \bigg|_{t=0} = \frac{V_{om}}{\tau} = 2\pi f_t V_{om} \]

• If \( V_{om} > \frac{SR}{2\pi f_t} \), then the output is slew-rate limited and changes linearly, not exponentially. Also \( v_n \neq v_p \).

• If gain is larger than 1, replace \( f_t \) with \( \beta f_t \) on the above expressions.

• Analysis shows that \( f_t \approx \frac{g_{m1}}{2\pi C_C} \), so \( C_C = \frac{g_{m1}}{2\pi f_t} \), and

\[ SR = \frac{I_A}{C_C} = \frac{2\pi f_t I_A}{g_{m1}} \]
• SR can be increased by increasing $I_A$.

• SR can be increased by decreasing $g_m$ using a FET input stage or adding resistors to the differential stage’s emitter (emitter degeneration).

• Using opamps with higher $f_t$.

• Full-power bandwidth (FPB): maximum frequency at which the opamp will yield an undistorted sinusoidal output with the largest possible amplitude. Assuming saturation at $\pm V_{sat}$,

$$FPB = \frac{SR}{2\pi V_{sat}}$$

• Settling time: time it takes for the response to a large input step to remain within a specific error band. Example: AD843 will have $t_s = 135\text{ns}$ to 0.01% of a 10V step.