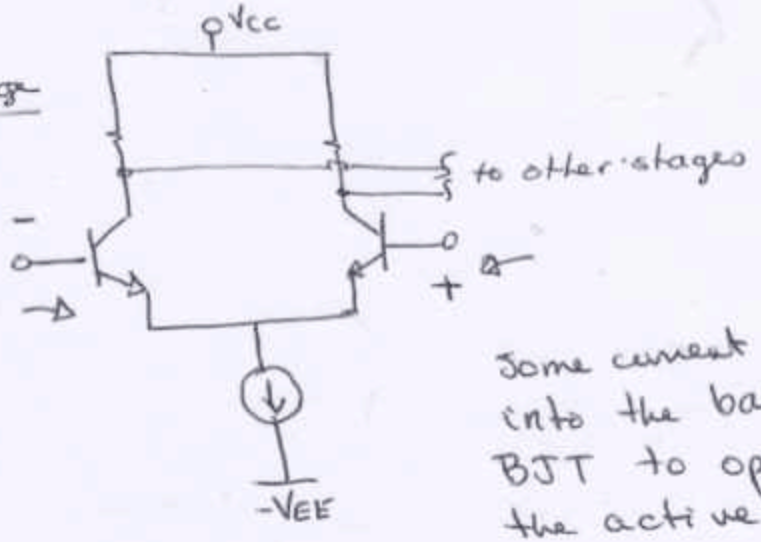
5207 - Lect. 6

Offsets → d.c. errors represented by voltages / currents

Due to errors in the manufacturing process or the the way transistors work (base currents for example)

Currents (Bias and Offset)

First stage



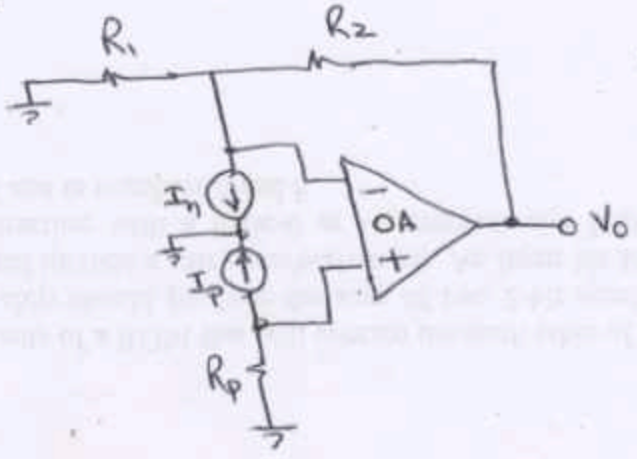
Some current must flow into the base for the BJT to operate in the active region

$$I_B = \frac{I_N + I_P}{2} \quad ; \quad I_{OS} = I_P - I_N$$

I_B → Needed by BJT to work. Sign is known.

I_{OS} → due to errors in manufacturing. Sign is not known.

A resistor R_p is added to cancel out the effect of I_B.



Superposition

V_o due to I_P: $(I_n = 0)$

$$V_+ = -I_P R_P$$

$$V_o = -\left(1 + \frac{R_2}{R_1}\right) I_P R_P$$

V_o due to I_N: $(I_P = 0)$

$$V_+ = 0 = V_- \Rightarrow i_{R_1} = 0$$ (gnd on both terminals)

$$V_O = + I_N R_2$$

Combined v_o:

$$V_o = -\frac{R_1 + R_2}{R_1} I_P R_P + I_N R_2$$

by definition $I_N + I_P = 2 I_B$

$I_P - I_N = I_{OS}$

$2 I_P = 2 I_B + I_{OS} \Rightarrow I_P = I_B + \frac{1}{2} I_{OS}$

$2 I_N = 2 I_B - I_{OS} \Rightarrow I_N = I_B - \frac{1}{2} I_{OS}$

$$V_O = I_B\left(R_2 - R_P \frac{R_1 + R_2}{R_1}\right) + \frac{1}{2} I_{OS}\left(R_2 + R_P \frac{R_1 + R_2}{R_1}\right)$$

I_B is typically one order of magnitude larger than I_{OS}.

If $R_2 = R_P \frac{R_1 + R_2}{R_1} \Rightarrow \boxed{R_P = \frac{R_1 R_2}{R_1 + R_2}}$

the effect of I_B is cancelled.

The error due to I_{OS} becomes

$$e_o = \frac{-1}{2} I_{OS} \left(R_2 + \frac{R_1 R_2}{R_1 + R_2} \frac{R_1 + R_2}{R_1} \right)$$

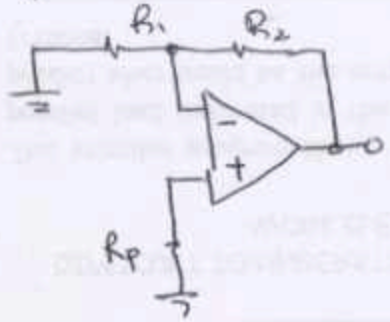
$$e_o = -R_2 I_{OS} = -\left(1 + \frac{R_2}{R_1}\right)(R_1 \| R_2)\, I_{OS}$$

↳ twice as large than if $R_P = 0$ but since $I_{OS} \sim I_B/10$ the total output error is reduced

Note: I_{OS} can be positive or negative, so sign of e_o is not known.

I_{OS} → specified in data sheet is the maximum ~~ideal~~ absolute value that can be expected. The manufacturer guarantees that the actual I_{OS} will be smaller than the specified value, with + or - sign.

Example: P5.2



μA741C

$I_B = 80\,nA$ (typ.)

$I_{OS} = 20\,nA$ (typ.)

$A_V = 10\,V/V$

Find components so:

$e_o \le 10\,mV$

minimum power dissipation in resistors.

Low input-bias-current OA

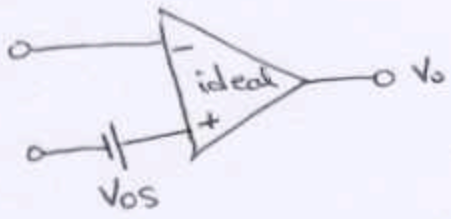
- Super beta
- Input bias current cancelation
- JFET - input OA
- MOSFET - input OA

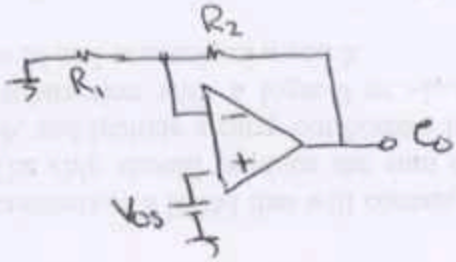
Changes in I_B with temperature

* ——————————— *

Input offset voltage → connecting both OA inputs together produces an output voltage ≠ 0

V_{OS} = input offset voltage
= correction that must be applied between the input pins to drive $V_o \to 0V$





$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_{OS}$$

V_{OS} changes with:

- Temperature (Thermal drift)

$$TC(V_{OS}) = \frac{\partial V_{OS}}{\partial T}$$

to take this into account, use

$$V_{OS}(T) = V_{OS}(25°C) + TC_{V_{OS}}(T - 25°C)$$

- CMRR → common-mode signal

The effect of a signal common to both inputs on the output is characterized with a parameter called the "common-mode rejection ratio".

$$\frac{\partial V_{OS}}{\partial V_{CM}} = \frac{1}{CMRR}$$

∴ change in V_{OS} due to the presence of a common-mode signal = $\Delta V_{OS_{CM}}$

$$\Delta V_{OS_{CM}} = \frac{1}{CMRR} V_{CM}$$

use $V_{CM} \simeq V_p$ for calculations

Example 5.4

Power-supply rejection ratio

$$\frac{1}{PSRR} = \frac{\partial V_{OS}}{\partial V_S} \quad ; \; V_S = \text{supply voltage}$$

Change in V_{OS} with output swing $= \frac{\Delta V_O}{a}$

a = open-loop gain of OA

$$V_{OS} = V_{OS\phi} + TC_{VOS} \times \Delta T + \frac{\Delta V_P}{CMRR} + \frac{\Delta V_S}{PSRR} + \frac{\Delta V_O}{a}$$

P. 5.12

P. 5.27