

PASS-TRANSISTOR LOGIC

INEL 4207 - Spring 2012

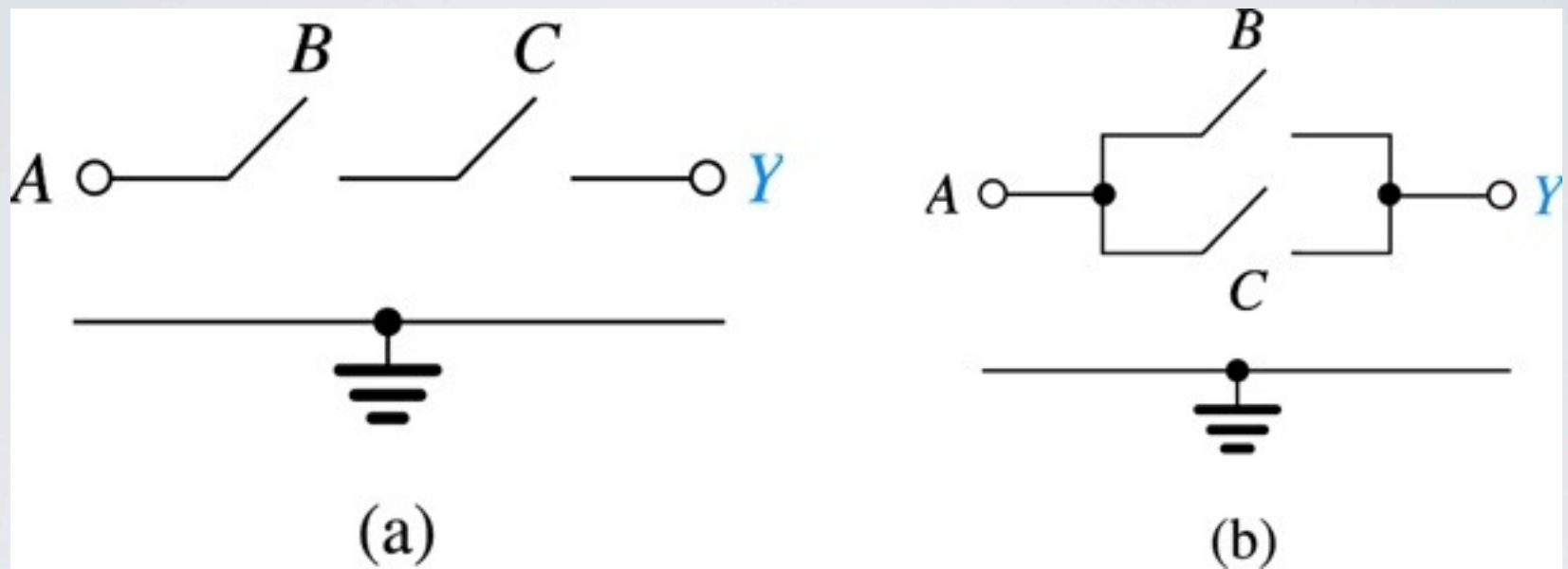


Figure 15.5 Conceptual pass-transistor logic gates. (a) Two switches, controlled by the input variables B and C , when connected in series in the path between the input node to which an input variable A is applied and the output node (with an implied load to ground) realize the function $Y = ABC$. (b) When the two switches are connected in parallel, the function realized is $Y = A(B + C)$.

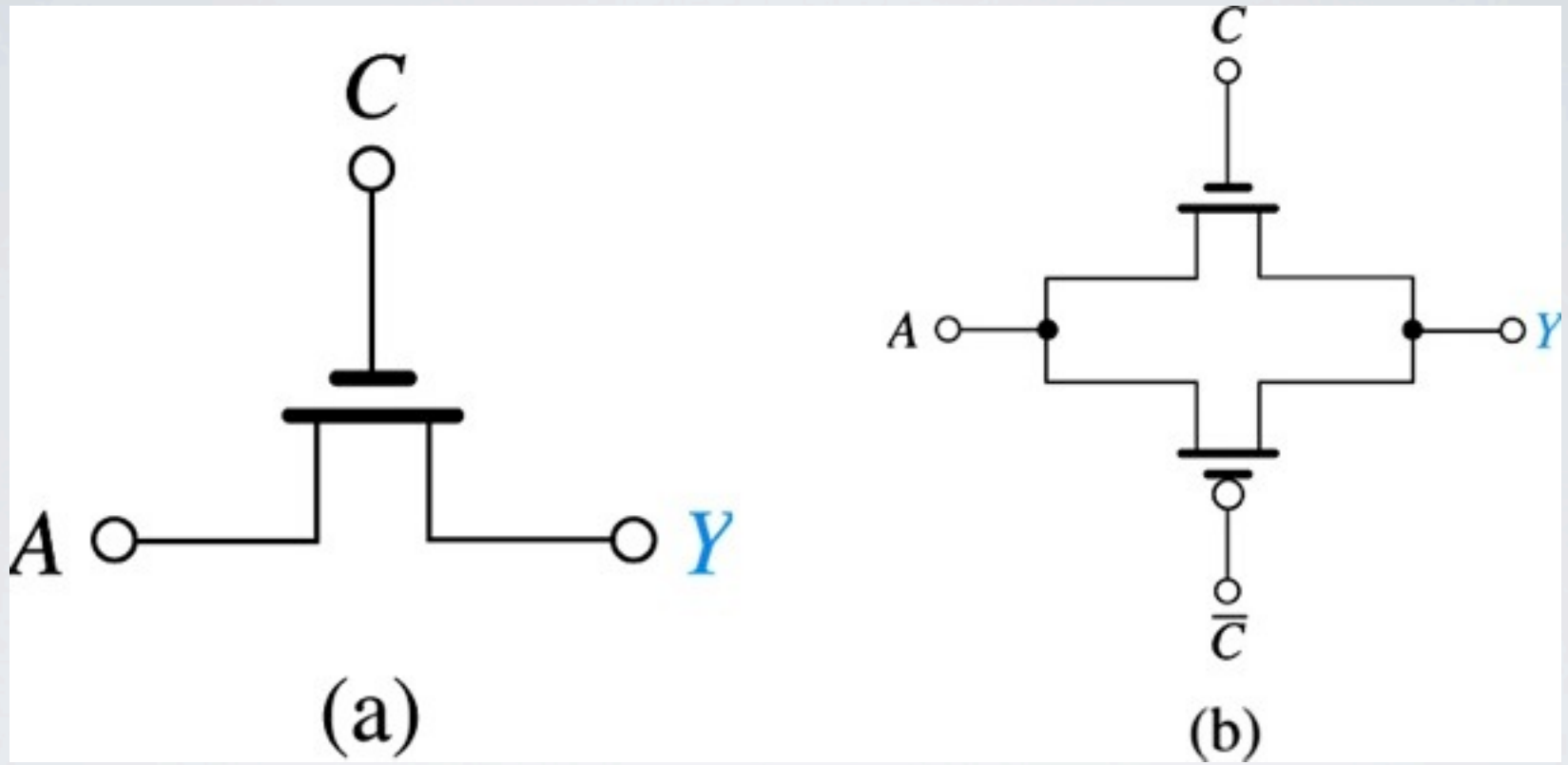


Figure 15.6 Two possible implementations of a voltage-controlled switch connecting nodes A and Y :
(a) single NMOS transistor and **(b)** CMOS transmission gate.

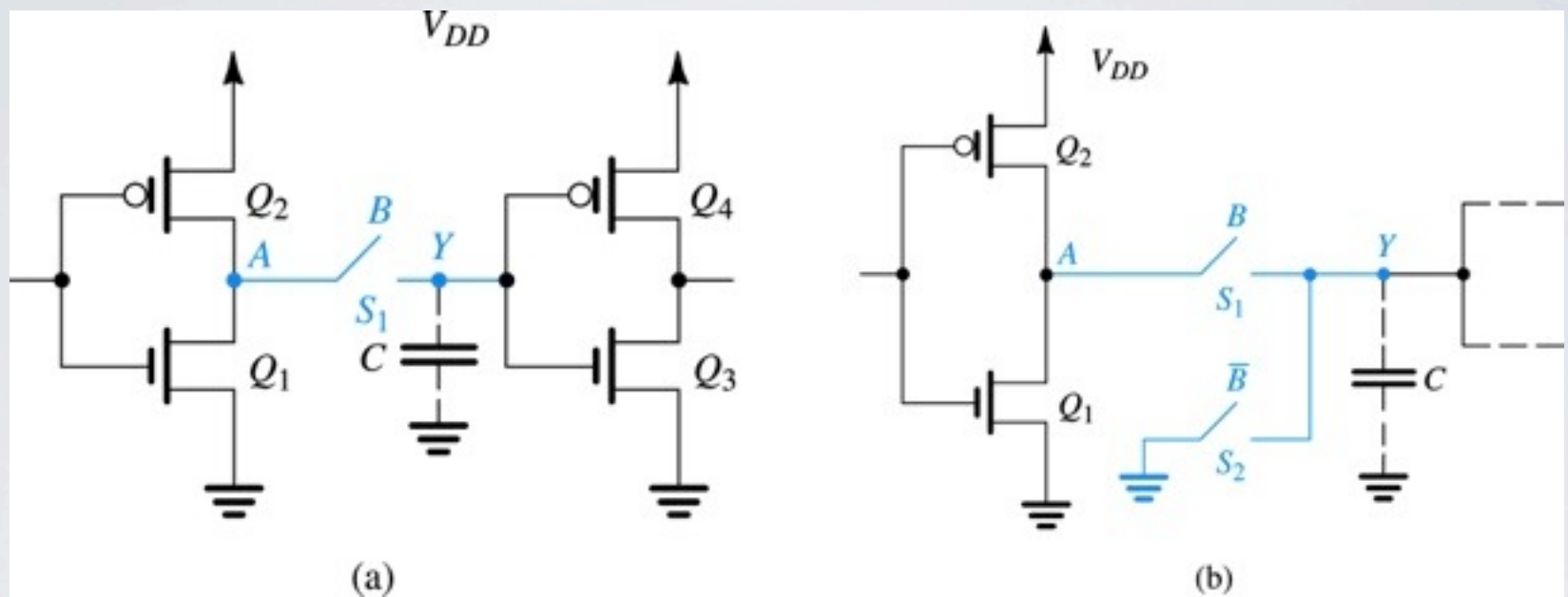
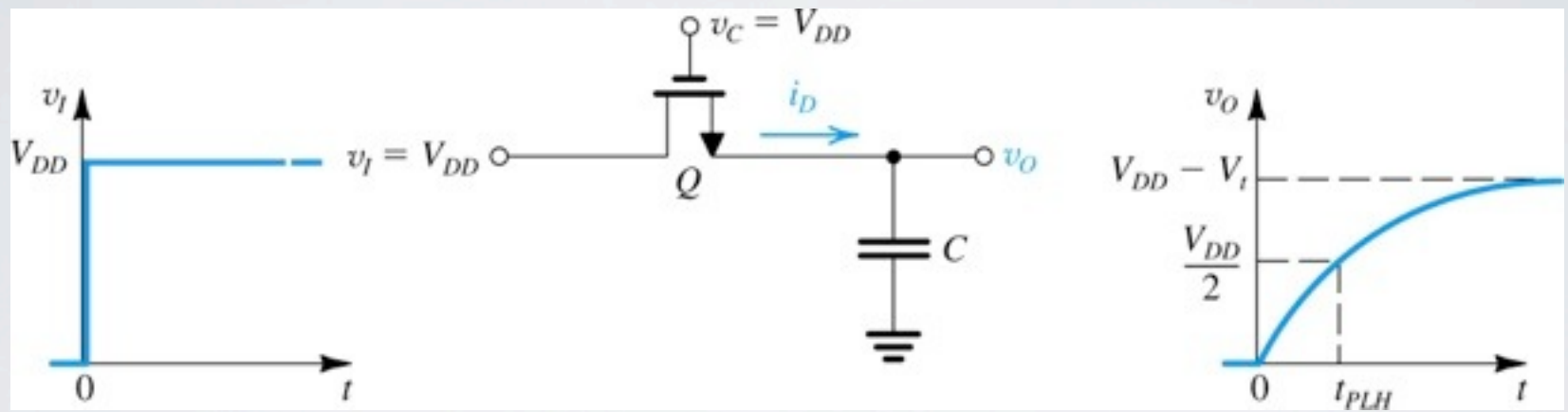


Figure 15.7 A basic design requirement of PTL circuits is that every node have, at all times, a low resistance path to either ground or V_{DD} . Such a path does not exist in (a) when B is low and S_1 is open. It is provided in (b) through switch S_2 .



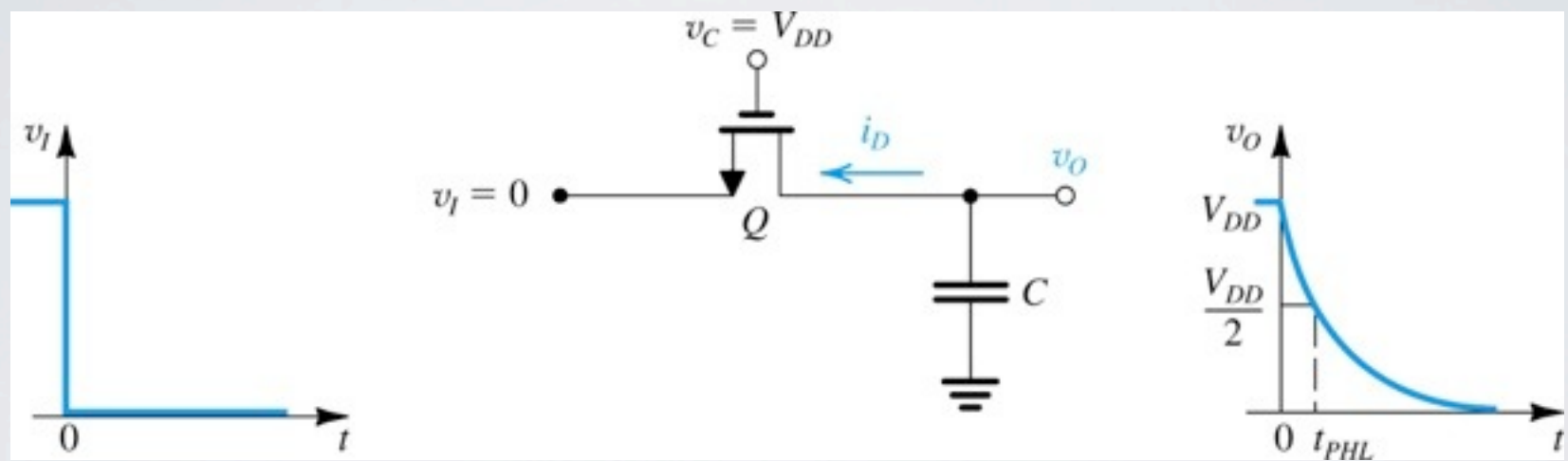


Figure 15.9 Operation of the NMOS switch as the input goes low ($v_I = 0$ V). Note that the drain of an NMOS transistor is always higher in voltage than the source; correspondingly, the drain and source terminals interchange roles in comparison to the circuit in Fig. 15.8.

Example

Consider the NMOS switch shown in figs. 15.8 and 15.9 for which $\mu_n C_{ox} = 50 \mu A/V^2$, $\mu_p C_{ox} = 20 \mu A/V^2$, $|V_{t0}| = 1V$, $\gamma = 0.5\sqrt{V}$, $2\phi_f = 0.6V$ and $V_{DD} = 5V$. Let the transistor have $W/L = 4\mu m/2\mu m$, and assume $C = 50fF$.

1. For v_i high, (fig. 15.8) find V_{OH} .
2. If the output feeds a CMOS inverter whose $(W/L)_p = 2.5(W/L)_n = 10\mu m/2\mu m$, find the static current in the inverter and its power dissipation when its input is the value found in (1). Find the inverter output voltage.
3. Find t_{PLH} .
4. Find t_{PHL} for the case with v_i going low (fig. 15.9).
5. Find t_p .

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Answer: (1) $V_{OH} = 3.4V$. (2) $i_{DP} = 18\mu A$, $P_D = 90\mu W$, $v_O = 0.08$. (3) $i_D(0) = 800\mu A$, $i_D(t_{PLH}) = 50\mu A$, $i_{D,AV} = 425\mu A$, $t_{PLH} = C(V_{DD}/2)/i_{D,AV} = 0.29ns$. (4) $t_{PHL} = 0.17ns$. (5) $t_p = 0.23ns$.

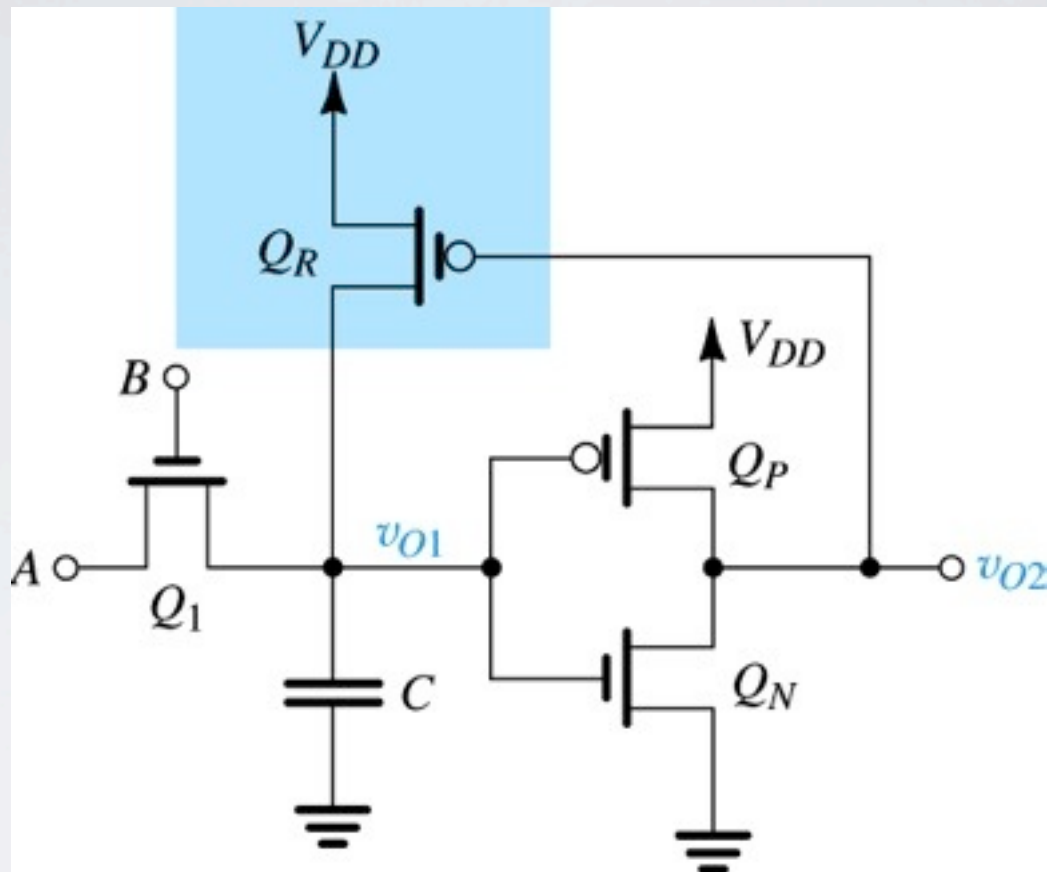


Figure 15.10 The use of transistor Q_R , connected in a feedback loop around the CMOS inverter, to restore the V_{OH} level, produced by Q_1 , to V_{DD} .

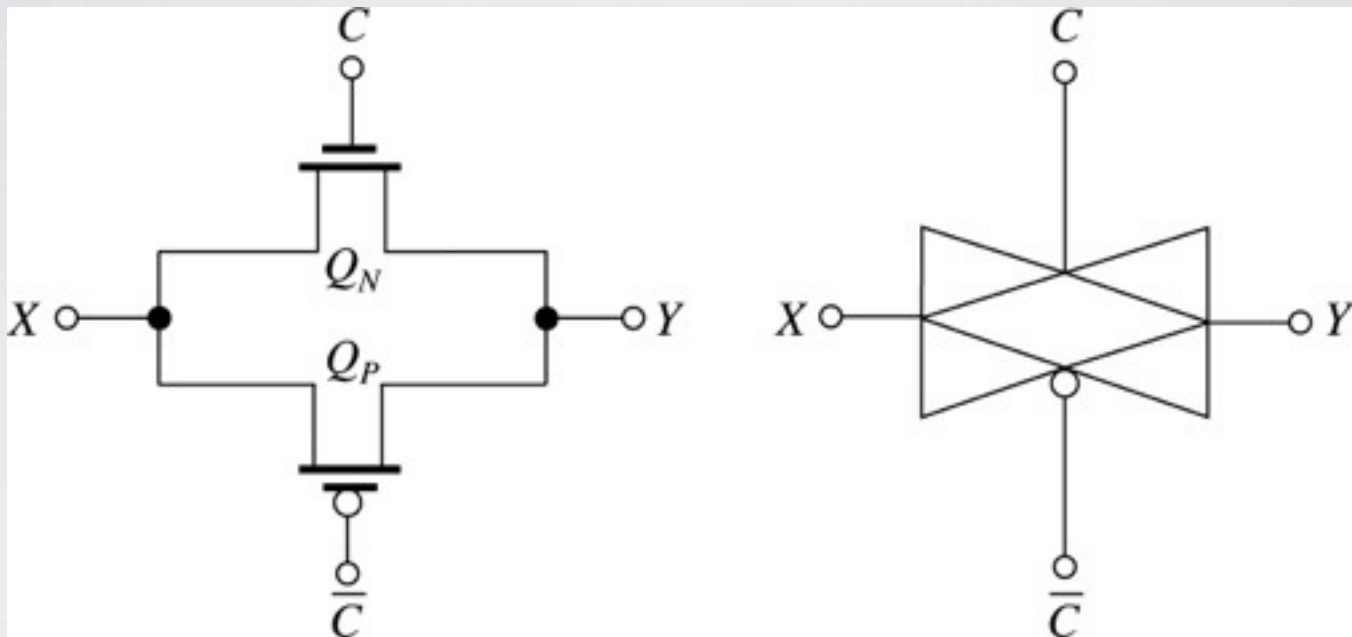
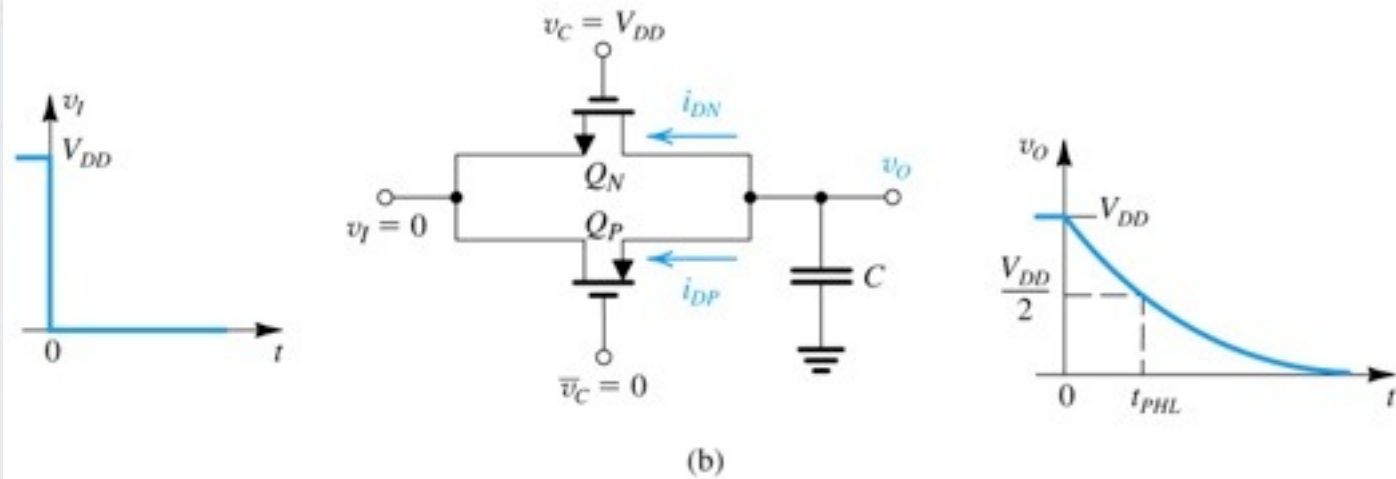
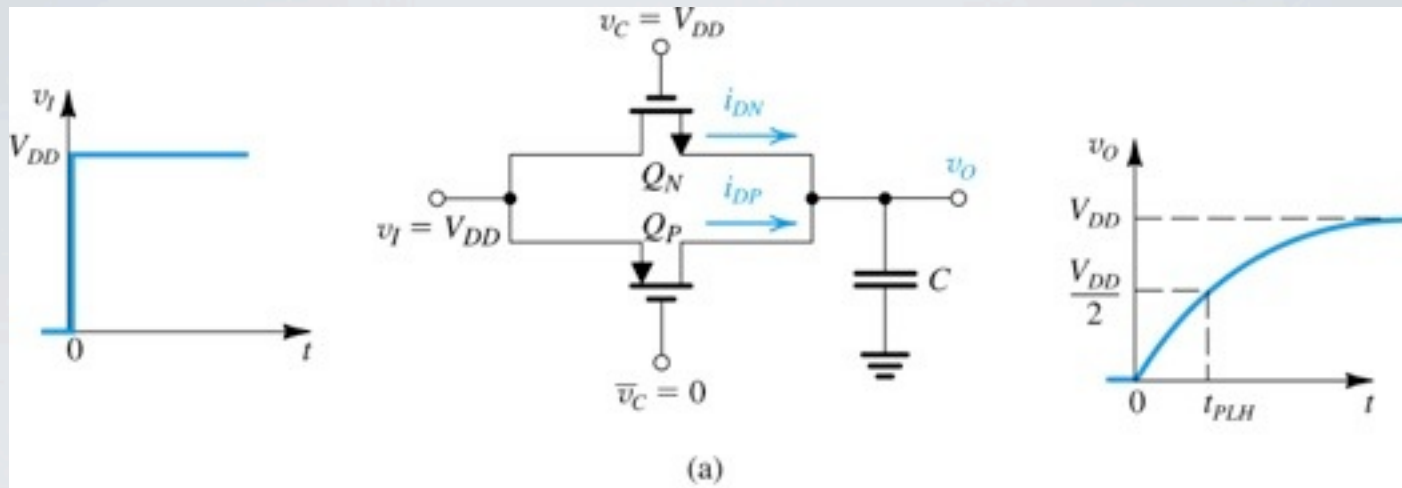
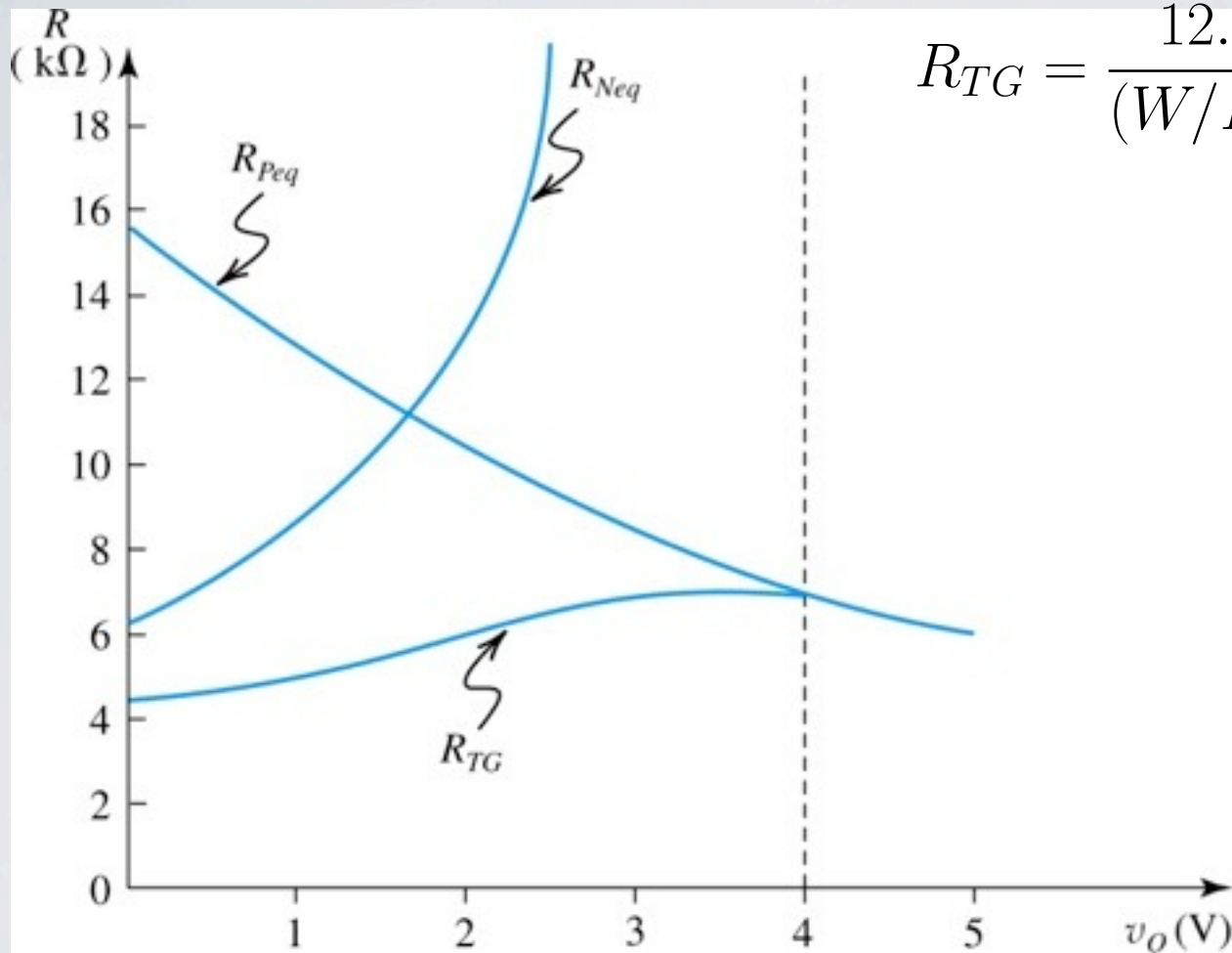


Figure 15.11 The CMOS transmission gate and its circuit symbol.



Transmission gate resistance empirical formula (for submicron technologies) (eq. 15.36)



$$R_{TG} = \frac{12.5}{(W/L)_n} k\Omega$$

Figure 15.13 Plot of the equivalent resistances of the two transistors of the transmission gate in Fig. 15.12(a) and the overall resistance R_{TG} versus v_O . The data apply to the situation specified in Exercise 15.5.

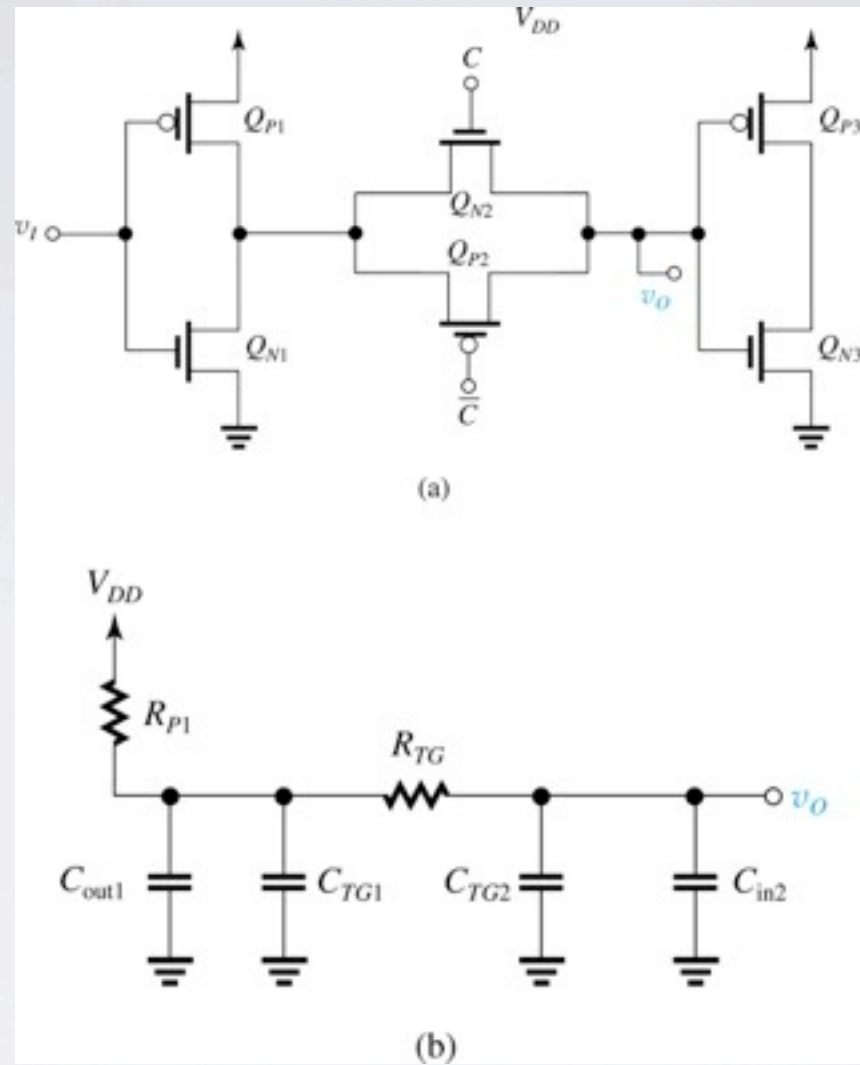


Figure 15.14 (a) A transmission gate connects the output of a CMOS inverter to the input of another. (b) Equivalent circuit for the purpose of analyzing the propagation delay of the circuit in (a).

Elmore delay formula (eq. 15.37):

$$t_p = 0.69 [C_1 R_1 + C_2 (R_1 + R_2) + C_3 (R_1 + R_2 + R_3)]$$

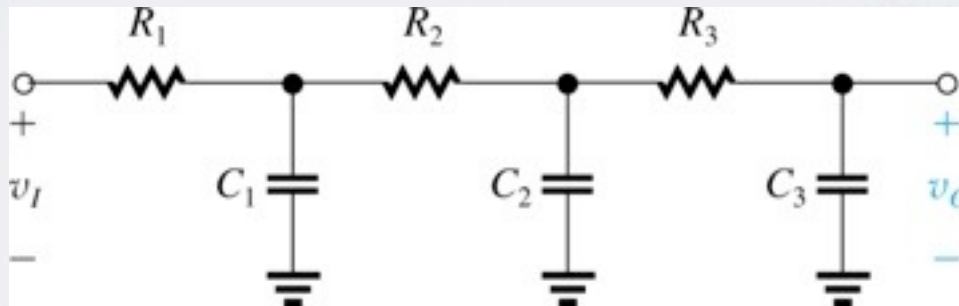
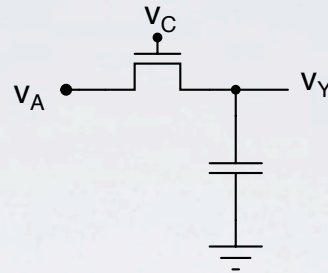


Figure 15.15 A three-section RC ladder network.

For the circuit if fig. 15.14, fabricated using $0.13\mu m$ technology, Q_p of the first inverter has $W/L = 2$, and both transistors in the t.g. have $W/L = 1$. The caps are $C_{out1} = 10fF$, $C_{TG1} = C_{TG2} = 5fF$, and $C_{in2} = 10fF$. Use empirical formulas to obtain R_{P1} and R_{TG} ; then find t_p .

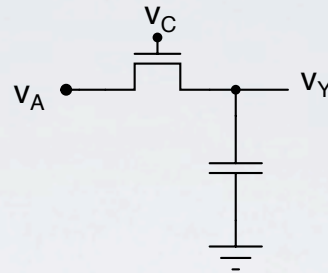
2. The following diagram shows an NMOS transistor operating as a switch.



Assuming that $\mu_n C_{ox} = 300 \mu A/V^2$, $W/L = 1.5$, $V_{t0} = 1V$, $\gamma = 0.5V^{1/3}$, and $2\phi_F = 0.6V$, find

- (a) the maximum voltage across the capacitor, v_Y , if $v_A = v_C = 5V$. (15 pts)
- (b) the voltage that must be applied to v_C so that the voltage across the capacitor, v_Y , reaches $5V$ if $v_A = 5V$. (10 pts)
- (c) an estimate of the fall time t_f that it takes for v_Y to drop from 90% to 10% of its initial value of $5V$, using the average current method. Assume $C = 1pF$, $v_A = 0V$ and $v_C = 5V$. (10 pts)

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Ans.: (a) $v_Y = 3.4V$; (b) $v_C = 6.8V$; (c) $i_{D1} = 3.6mA$; $i_{D2} = 0.84mA$; $t_f = 1.8ns$

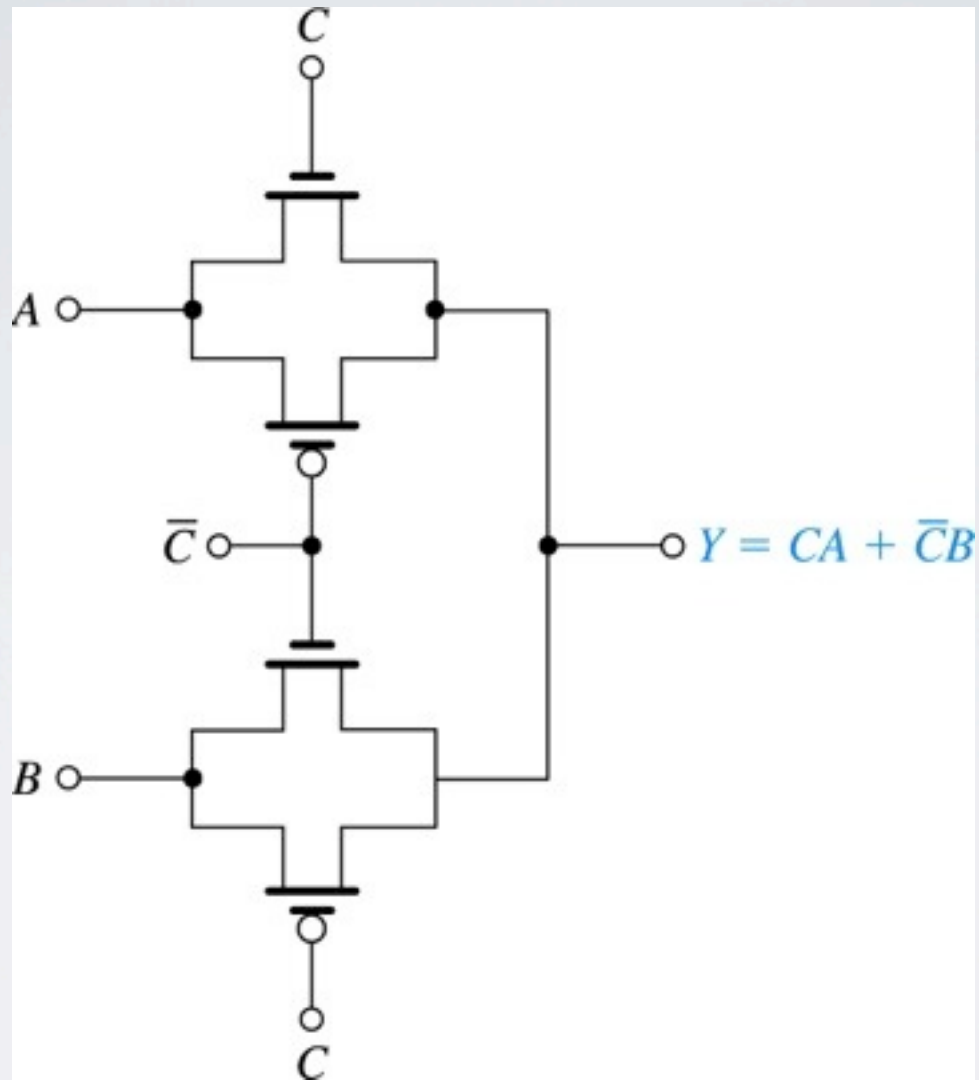


Figure 15.16 Realization of a two-to-one multiplexer using pass-transistor logic.

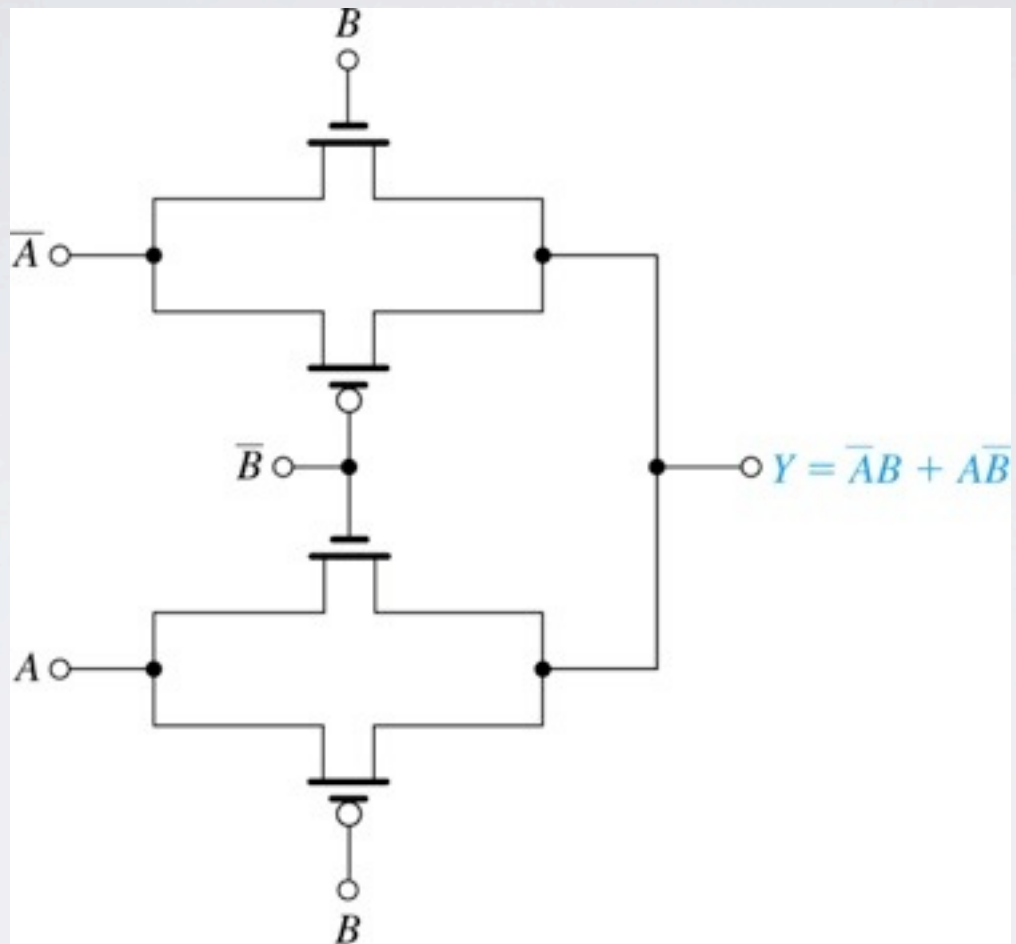


Figure 15.17 Realization of the XOR function using pass-transistor logic.

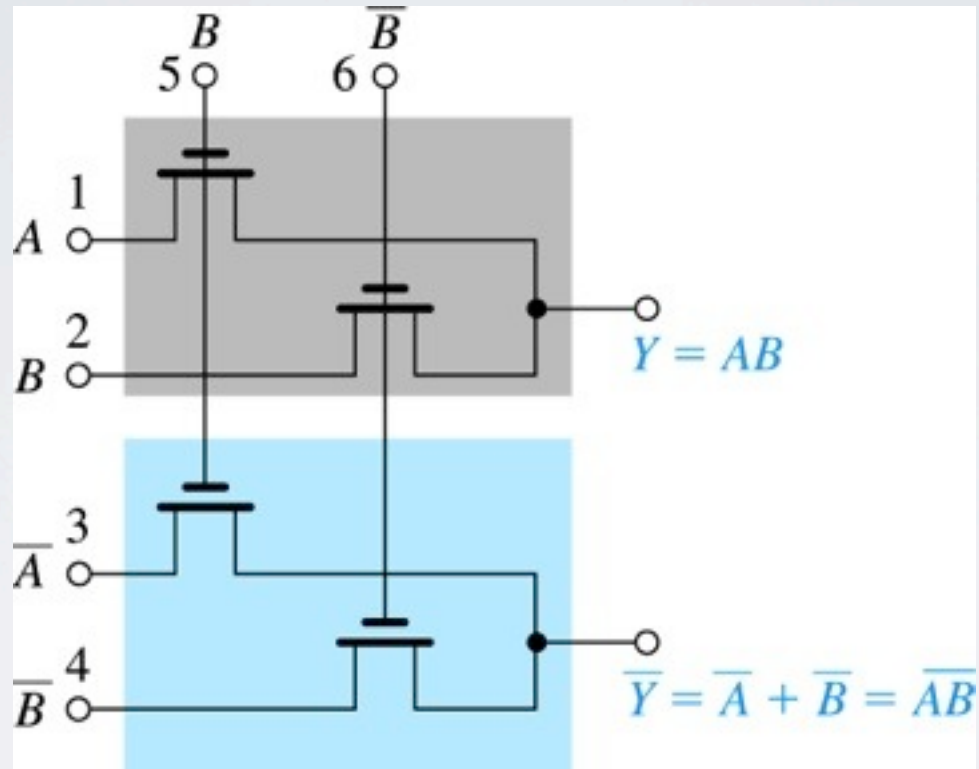


Figure 15.18 An example of a pass-transistor logic gate utilizing both the input variables and their complements. This type of circuit is therefore known as complementary pass-transistor logic, or CPL. Note that both the output function and its complement are generated.

Probs. 13, 16, 21

Dynamic Logic

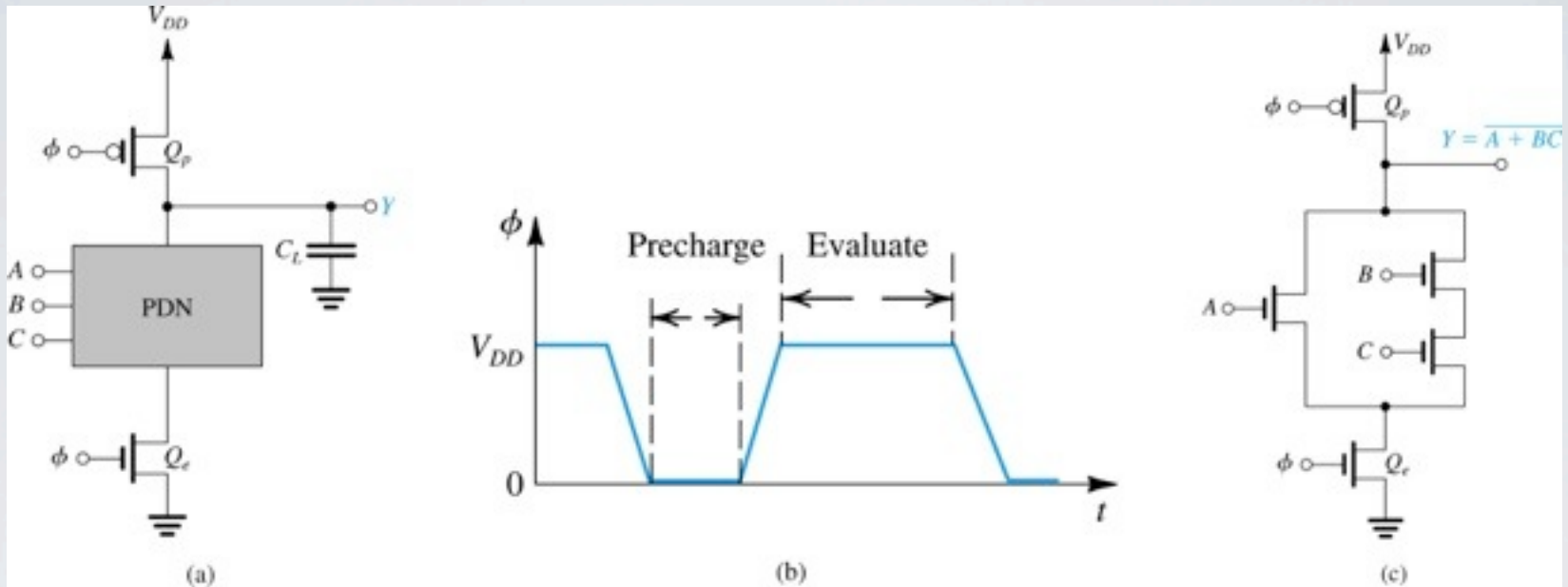


Figure 15.19 (a) Basic structure of dynamic-MOS logic circuits. (b) Waveform of the clock needed to operate the dynamic logic circuit. (c) An example circuit.