

Project

- 1 The project consists on the design and *SPICE* simulation of a 4-bit adder-subtractor, similar to the one shown in figure 4-13 of *Digital Design*, 4th edition, by Morris Mano.
- 2 Students will work in teams of 3 people.
- 3 Student will design the circuit and perform the simulation using individual transistors, organized in CMOS gates.
- 4 The simulation will use SPICE LEVEL 3 MOSFET model.
- 5 A parasitic capacitance of 1pF should be assigned to each interconnect.
- 6 Each team should deliver a report summarizing their work. The report should include the following:
  - a. Title page with student name and number
  - b. Description of the problem
  - c. Description and theoretical analysis of the circuit, specifically describing how it works, what are the expected levels of performance in terms of propagation speed and power dissipation
  - d. Results of the SPICE simulation, and a comparison with the analytical results.
- 7 The report is due on April 7, 2011.