Memory Circuits

Latches and flip-flops

INEL 4207 - Fall 2011

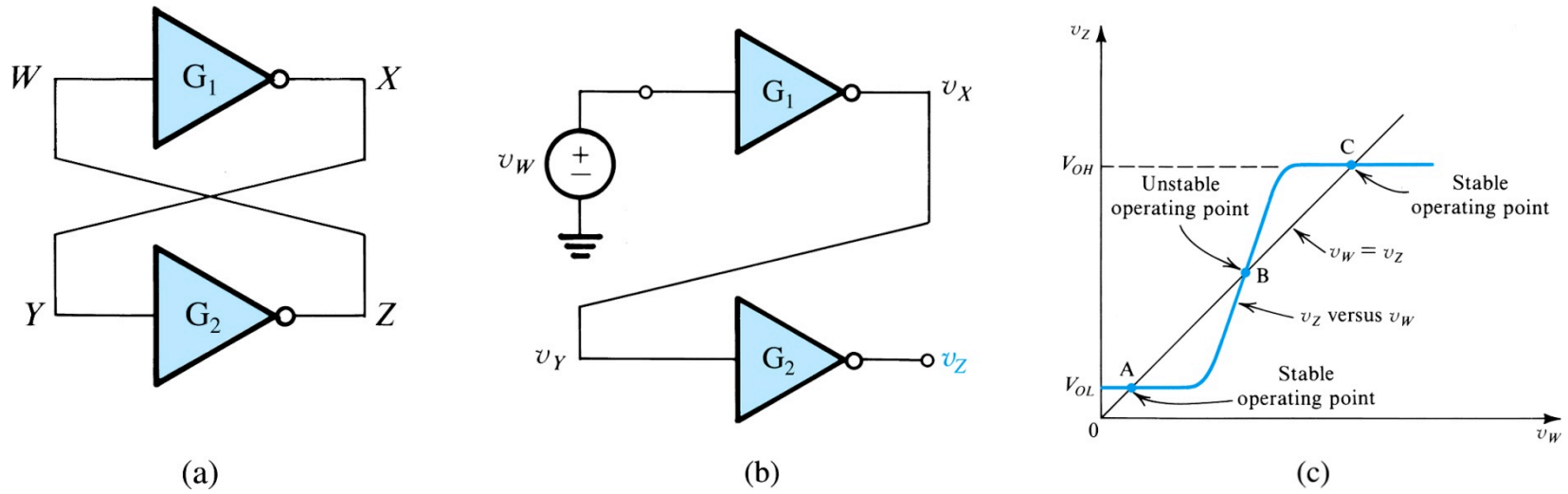


Figure 16.1 (a) Basic latch. (b) The latch with the feedback loop opened. (c) Determining the operating point(s) of the latch.

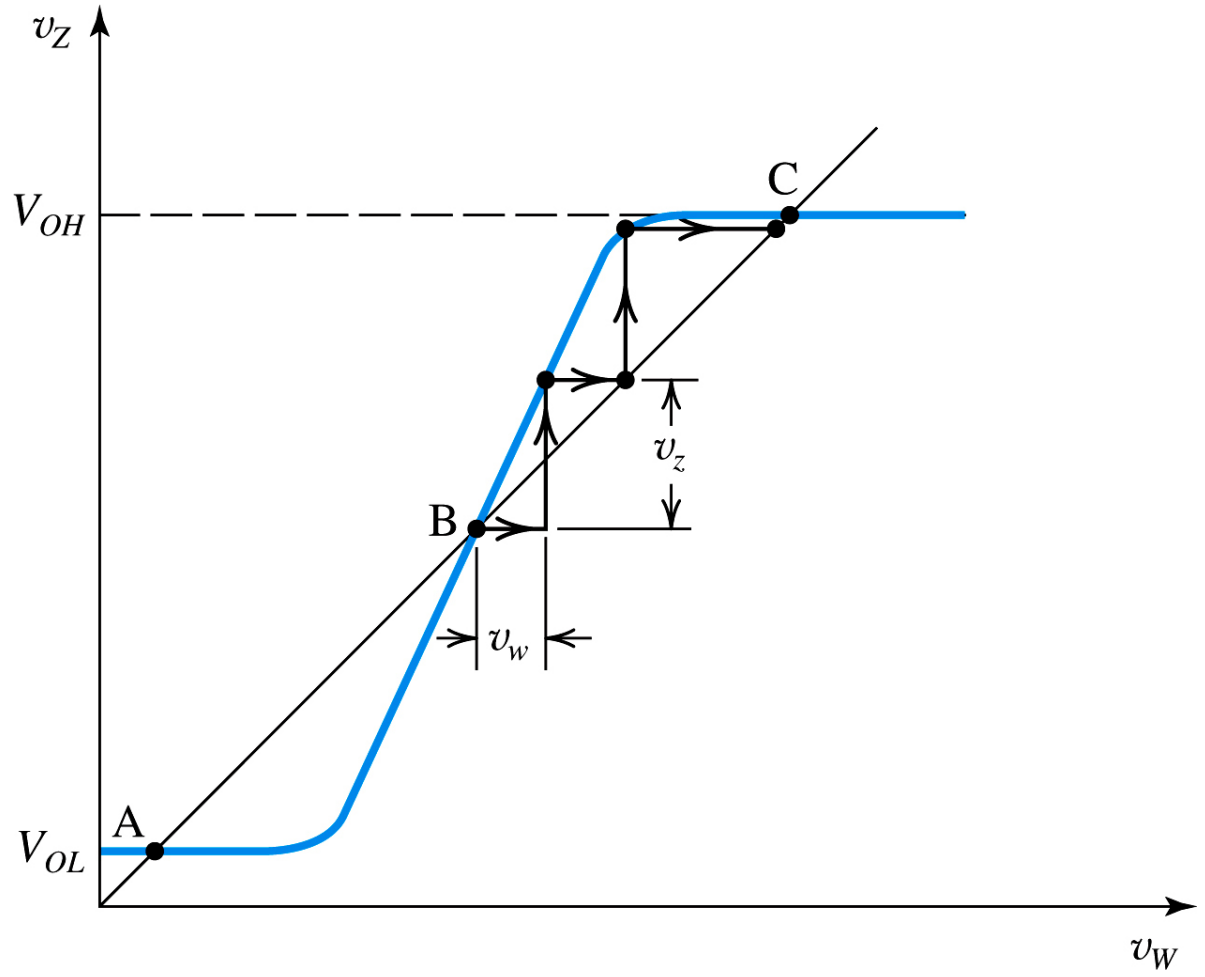
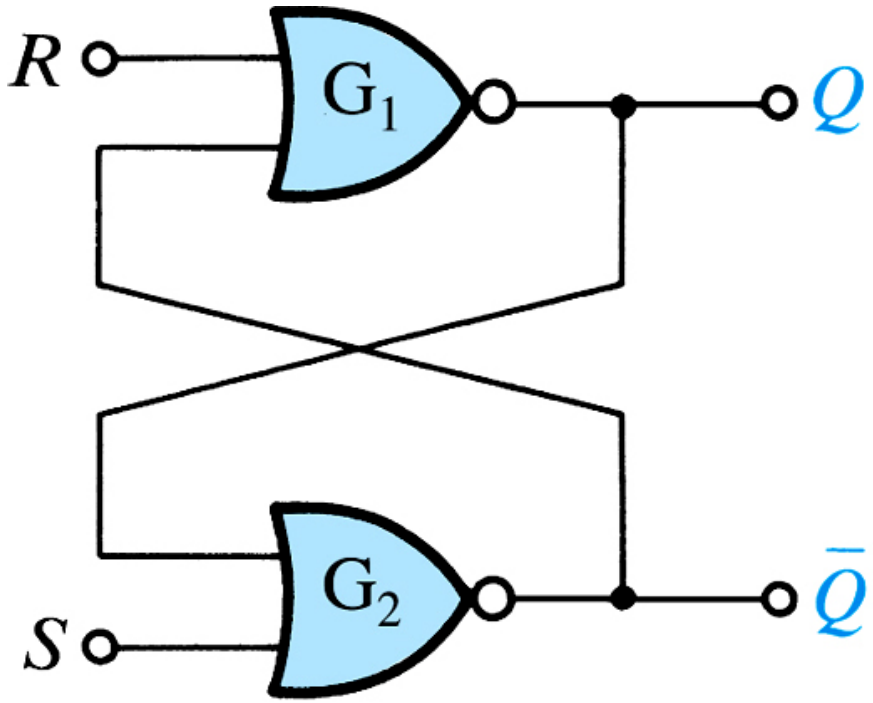


Figure 16.2



(a)

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	Not used

(b)

Figure 16.3 (a) The set/reset (SR) flip-flop and (b) its truth table.

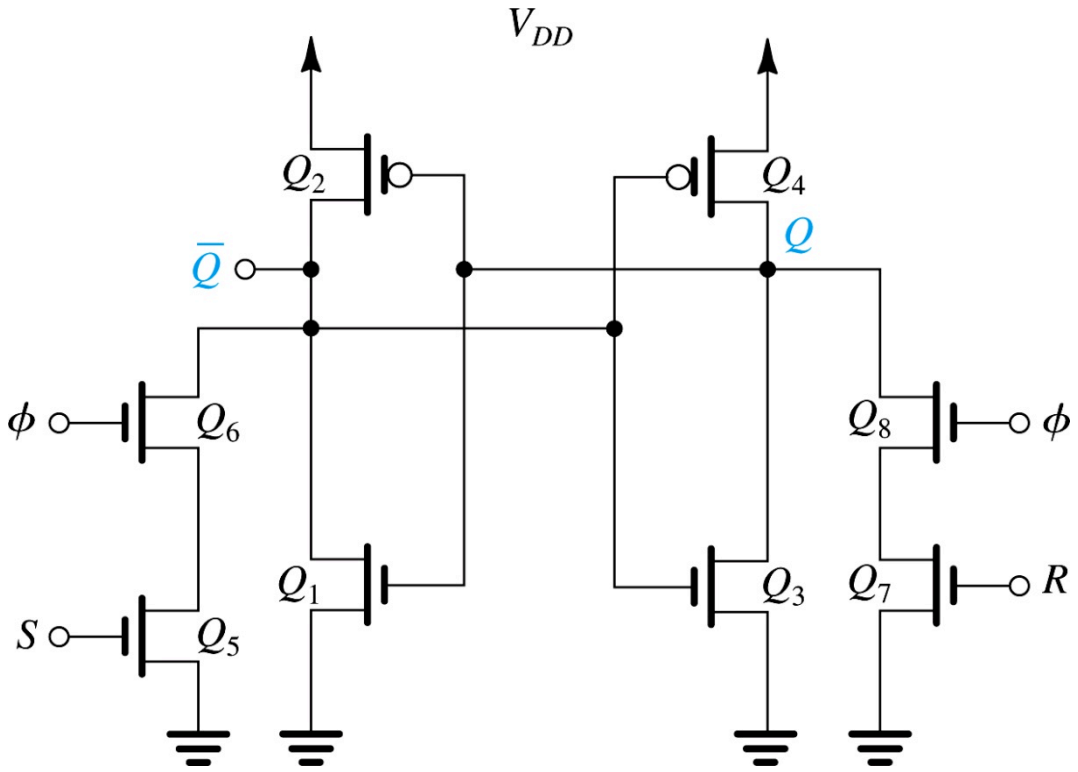


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

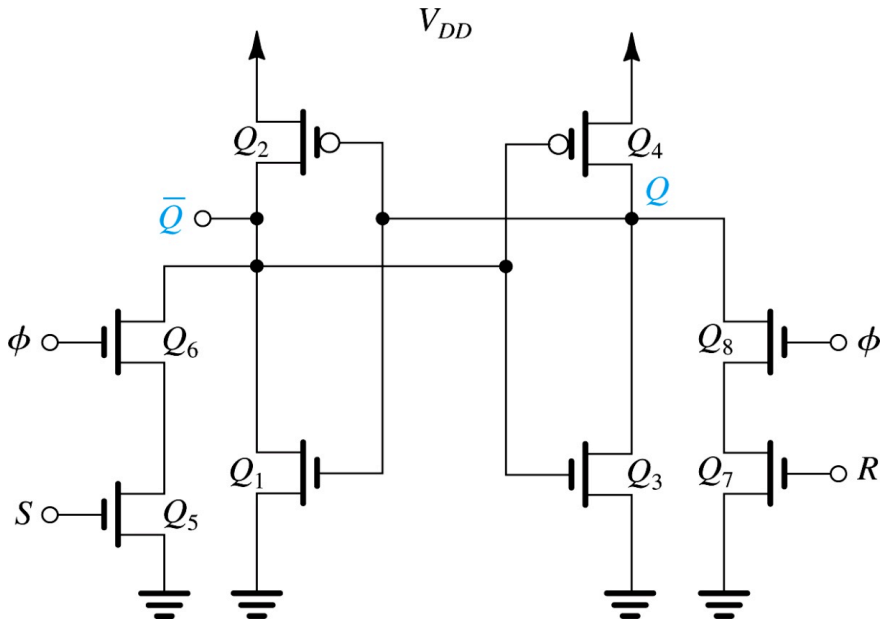


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

1. Assume Q=0, Q' = 1
2. Clock and S go high
3. Q' is pulled down
4. Inv Q_3/Q_4 -> reaches transition point ($V_{DD}/2$)
5. Inv Q_3/Q_4 -> regenerative action forces Q_3 into cutoff
6. Inv Q_1/Q_2 -> reaches transition point ($V_{DD}/2$)
7. Regenerative action keeps Q' low even if S goes low

Example 1

The CMOS SR flip-flop in Fig. 16.4 is fabricated in a 0.18-μm process for which $\mu_n C_{ox} = 4\ \mu_p C_{ox} = 300\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5V$, and $V_{DD} = 1.8V$. The inverters have $(W/L)_n = 0.27\mu m/0.18\mu m$ and $(W/L)_p = 4\ (W/L)_n$. The four NMOS transistors in the set-reset circuit have equal W/L ratios.

(a) Determine the minimum value required for this ratio to ensure that the flip-flop will switch.

(b) Also, determine the minimum width the set pulse must have for the case in which the W/L ratio of each of the four transistors in the set-reset circuit is selected at twice the minimum value found in (a). Assume that the total capacitance at each of the Q and $\overline{Q}$ nodes and ground is **20fF**.

Assume that initially Q = 0, Q' = 1

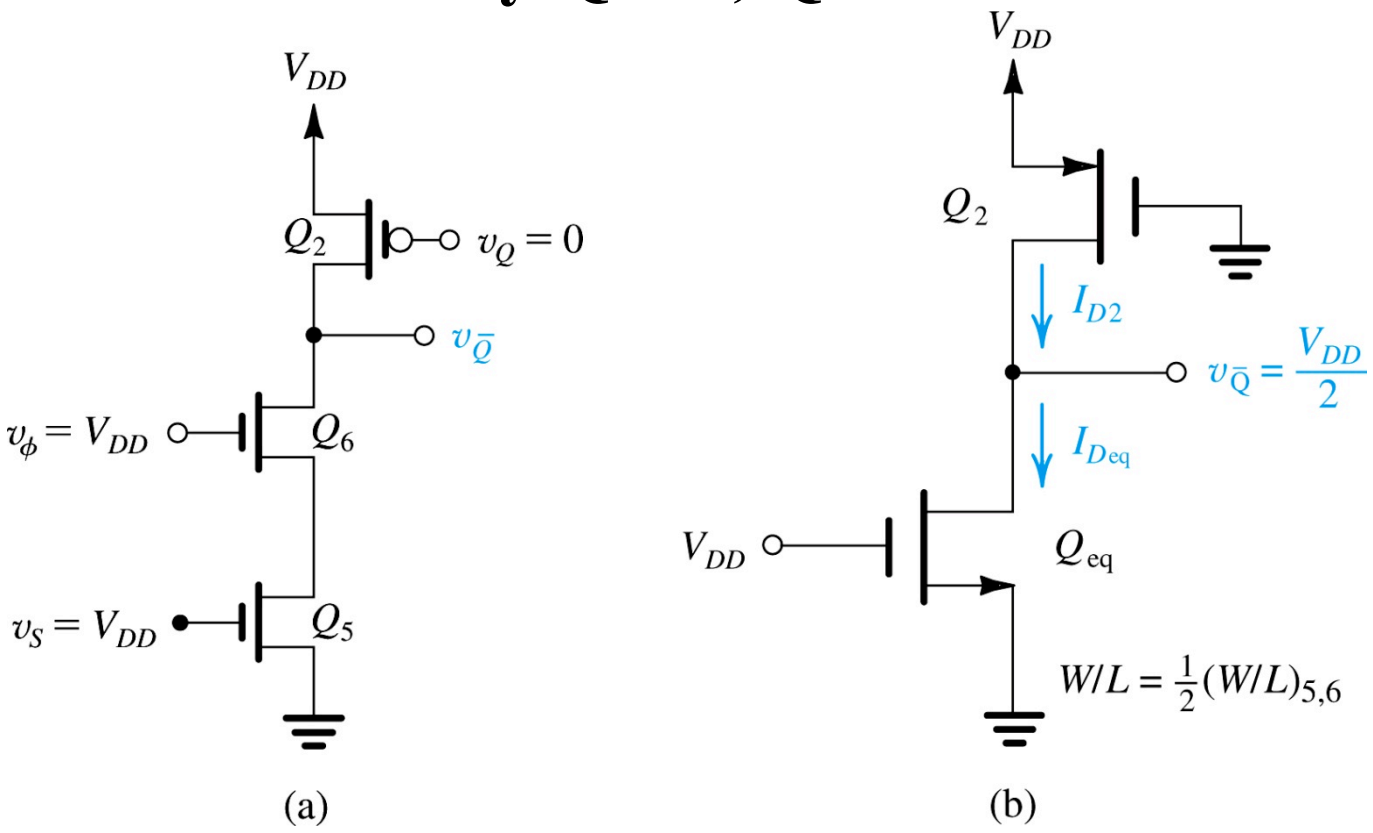


Figure 16.5 (a) The relevant portion of the flip-flop circuit of Fig. 16.4 for determining the minimum W_L ratios of Q_5 and Q_6 needed to ensure that the flip-flop will switch. (b) The circuit in (a) with Q_5 and Q_6 replaced with their equivalent transistor Q_{eq}, at the point of switching.

Assume that initially Q = 0, Q' = 1

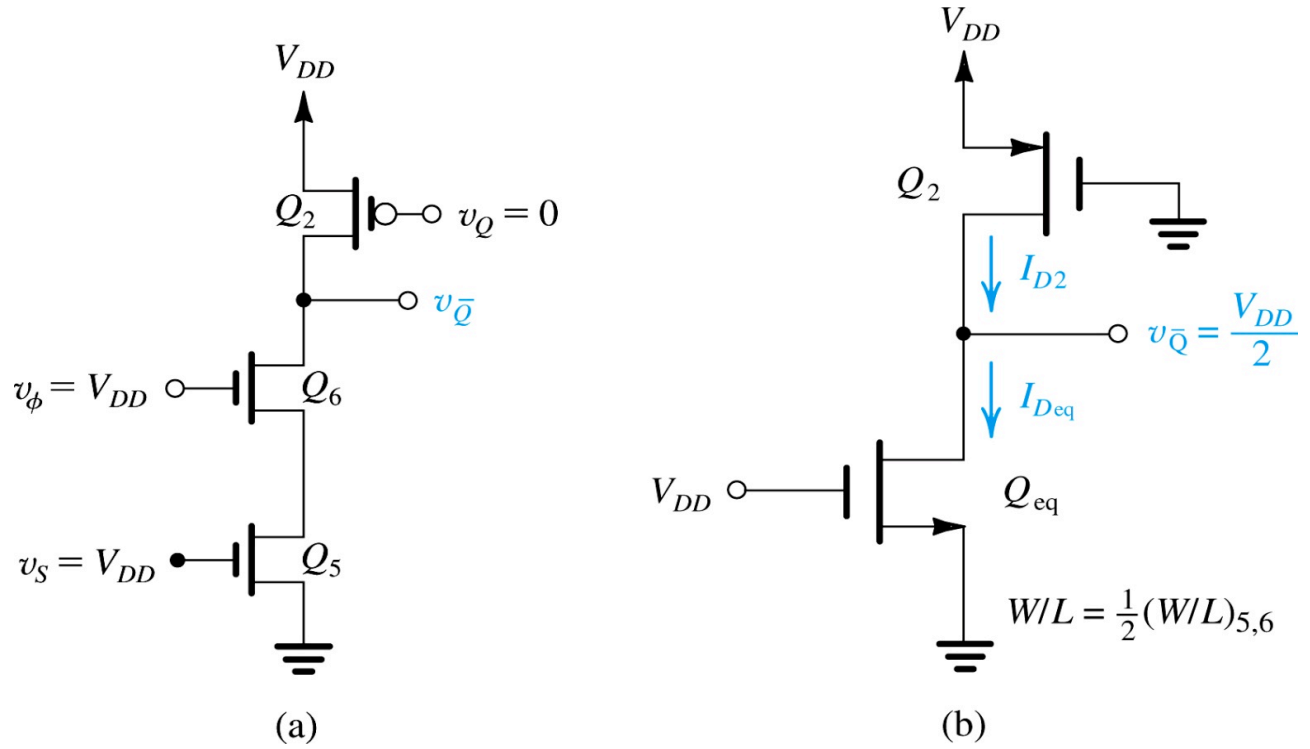


Figure 16.5 (a) The relevant portion of the flip-flop circuit of Fig. 16.4 for determining the minimum W_L ratios of Q_5 and Q_6 needed to ensure that the flip-flop will switch. (b) The circuit in (a) with Q_5 and Q_6 replaced with their equivalent transistor Q_{eq}, at the point of switching.

(a) ANSWER: $(W/L)_5 = (W/L)_6 = 0.54um/0.18um$

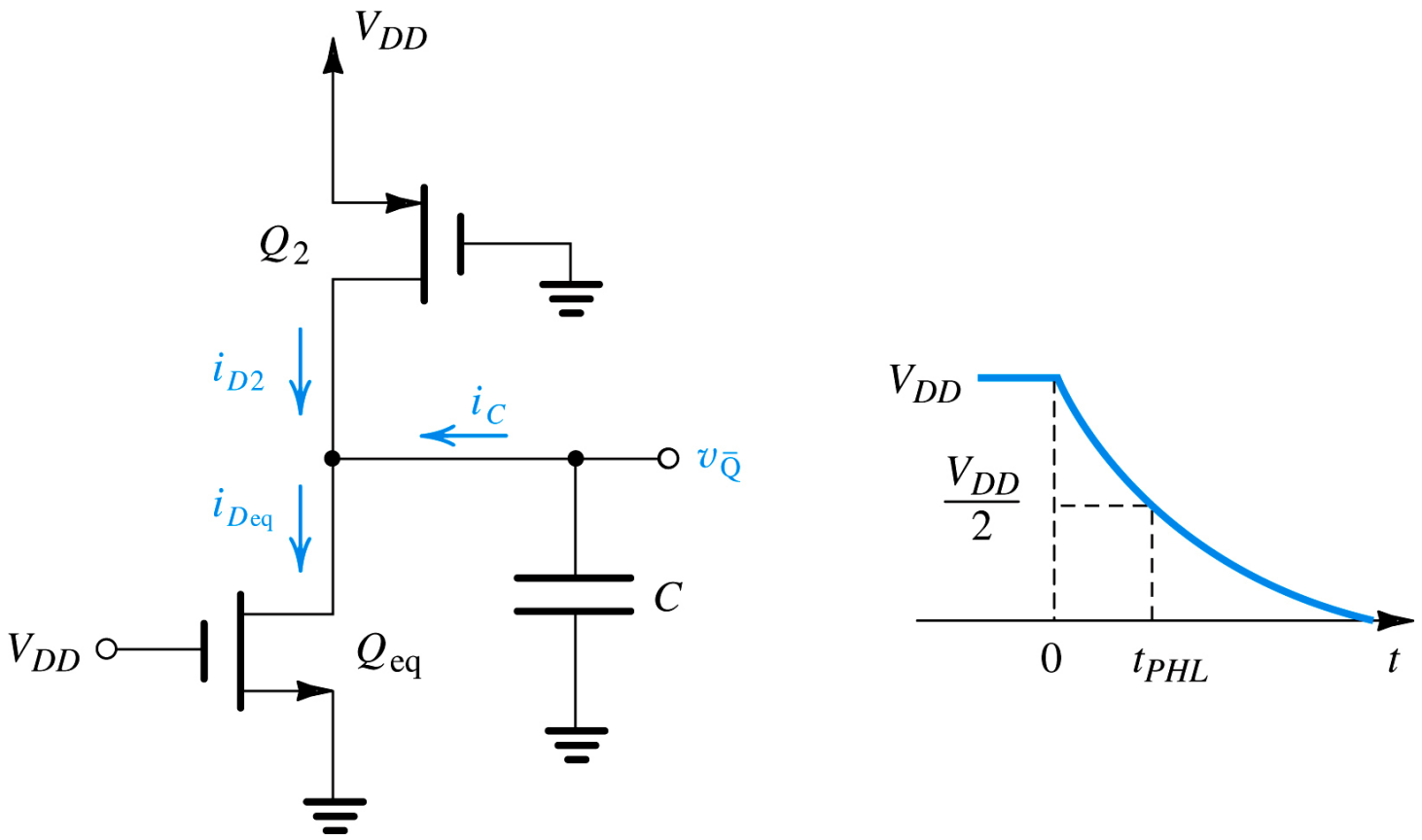


Figure 16.6 Determining the time t_{PHL} for $v_{\bar{Q}}$ to fall from V_{DD} to $V_{DD}/2$.

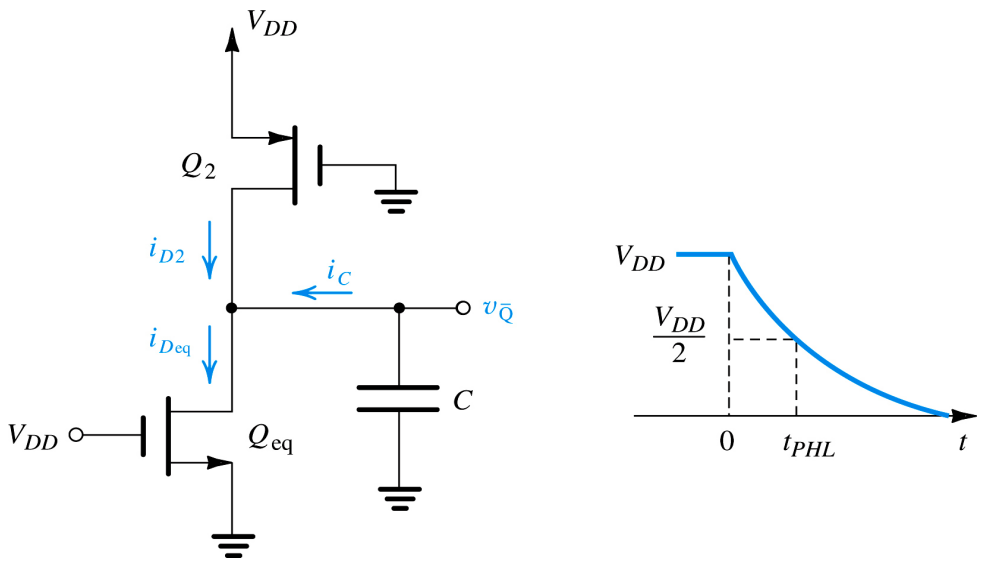


Figure 16.6 Determining the time t_{PHL} for $v_{\bar{Q}}$ to fall from V_{DD} to $V_{DD}/2$.

(b) ANSWER: Add t_{PHL} for Q1-Q2 and t_{PHL} for Q3-Q4. Set $(W/L)_5 = (W/L)_6 = (W/L)_7 = (W/L)_8$ = 1.08um/0.18um.

For Q_1-Q_2, use $i_C = i_{D,eq} - i_{D2}$. At t=0, $v_{Q'} = V_{DD}$ and Q_2 is off, Q_{eq} is saturated and i_C = 760.5uA. At t=t_{PHL}, $v_{Q'} = V_{DD}/2$ and i_{D2} = 344.25uA, i_{Deq} = 688.5uA and i_C = 344.25uA. i_{Cav} = 552.4uA, t_{PHL} = 32.6ps

For Q3-Q4, you can use the formulas from ch. 14 that use α to gat t_{PLH} = 49.5ps.

$T_{min} = t_{PHL} + t_{PLH}$

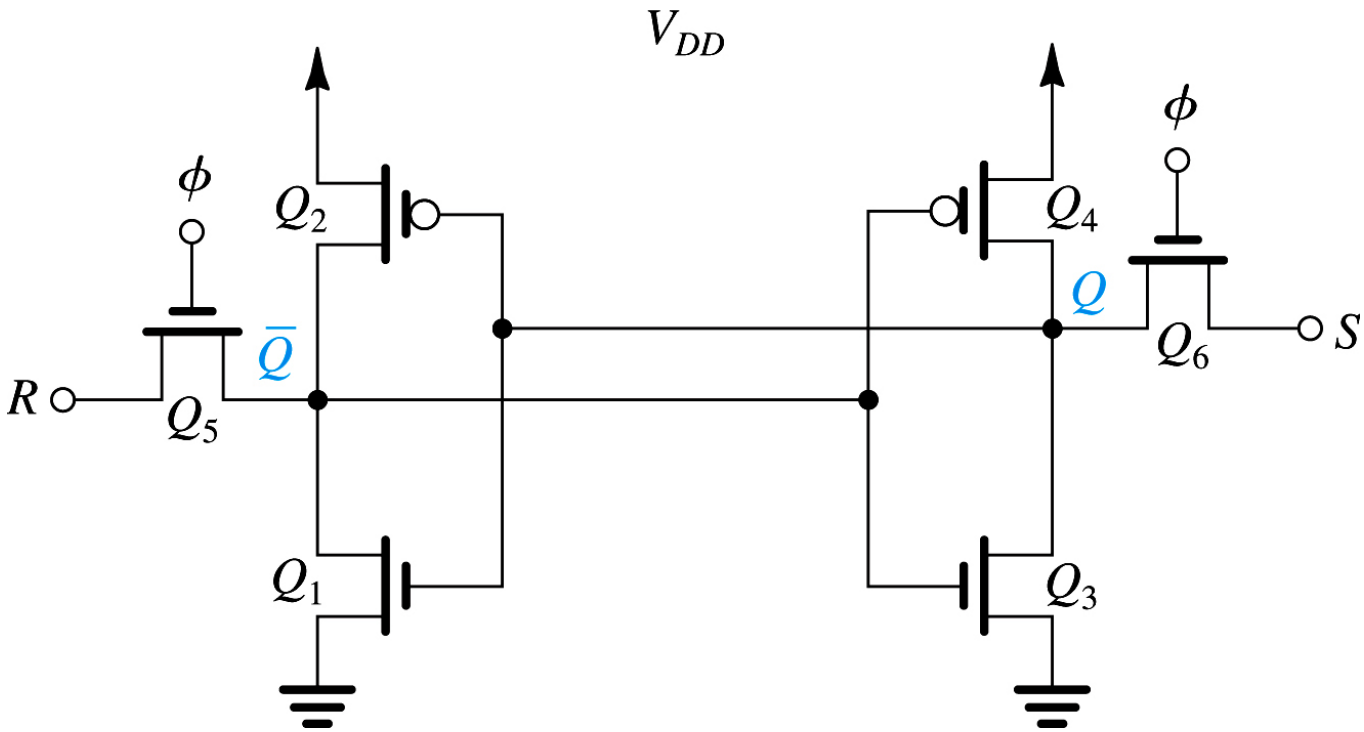


Figure 16.7 A simpler CMOS implementation of the clocked SR flip-flop. This circuit is popular as the basic cell in the design of static random-access memory (SRAM) chips.

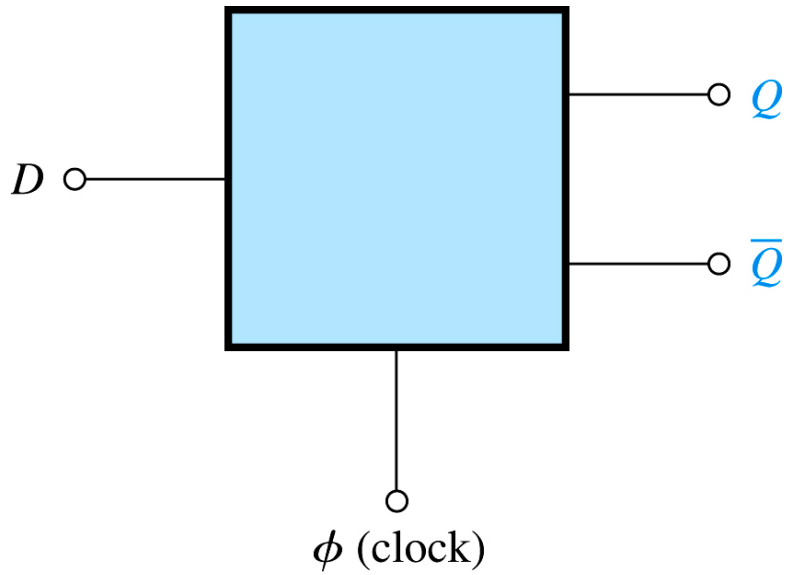


Figure 16.8 A block diagram representation of the D flip-flop.

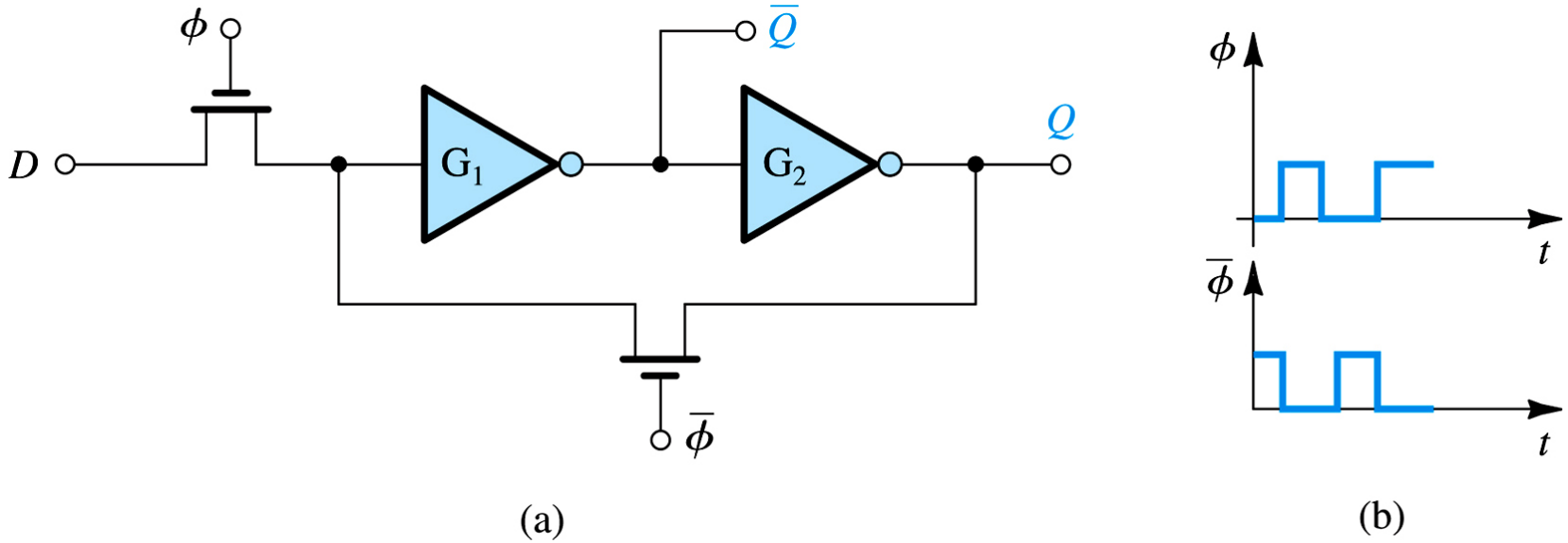


Figure 16.9 A simple implementation of the *D* flip-flop. The circuit in (a) utilizes the two-phase non-overlapping clock whose waveforms are shown in (b).

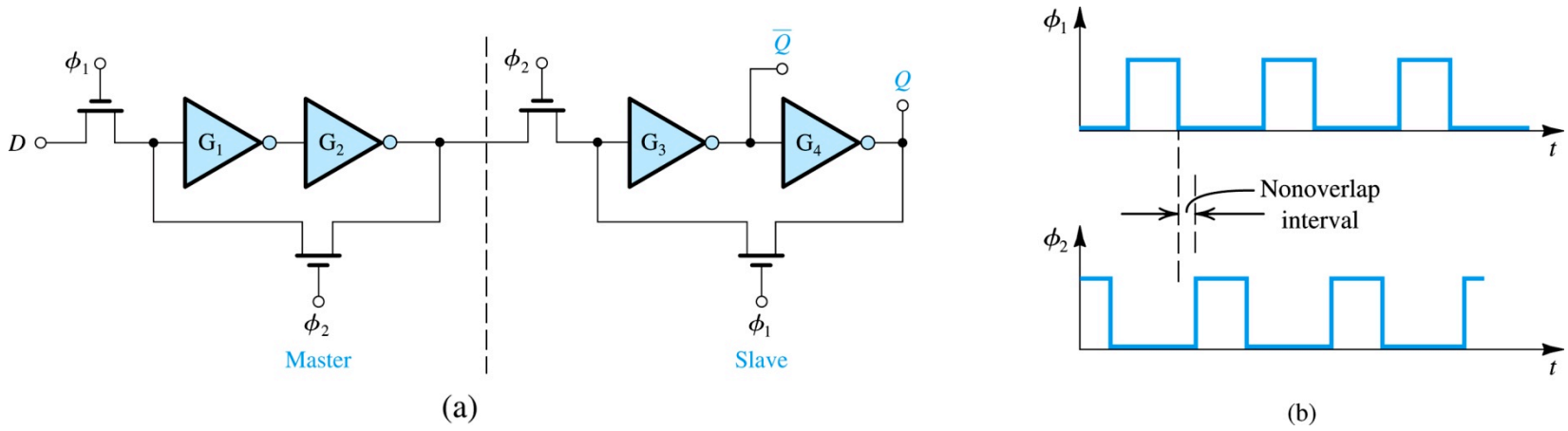


Figure 16.10 (a) A master–slave D flip-flop. The switches can be, and usually are, implemented with CMOS transmission gates. (b) Waveforms of the two-phase nonoverlapping clock required.