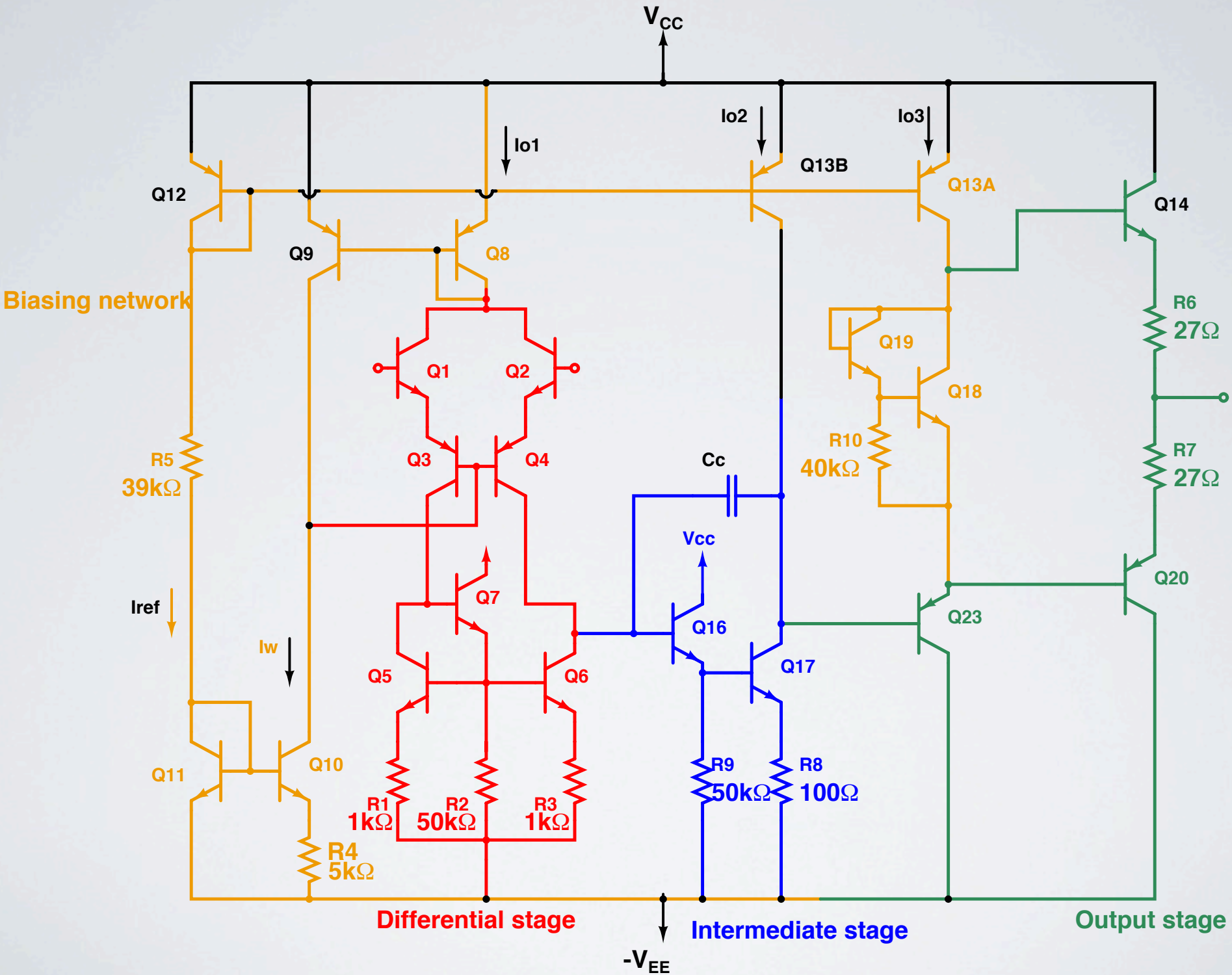
ANALYSIS OF THE UA741

INEL 4202 - Electronics II


V_{CC}
Io1
Io2
Io3
Q12
Q9
Q8
Q13B
Q13A
Q14
Biasing network
Q1
Q2
Q3
Q4
Q19
Q18
R6
27Ω
R10
40kΩ
R7
27Ω
R5
39kΩ
Cc
Vcc
Iref
Iw
Q7
Q16
Q20
Q23
Q5
Q6
Q17
Q11
Q10
R9
50kΩ
R8
100Ω
R1
1kΩ
R2
50kΩ
R3
1kΩ
R4
5kΩ
Differential stage
Intermediate stage
Output stage
$-V_{EE}$

- Standard npn transistors: $I_S = 10^{-14}A$ $\beta = 200$ $V_A = 125V$
- Standard pnp transistors: $I_S = 10^{-14}A$ $\beta = 50$ $V_A = 50V$
- Q_{13A}: $I_{SA} = 0.25 \times 10^{-14}A$
- Q_{13B}: $I_{SB} = 0.75 \times 10^{-14}A$

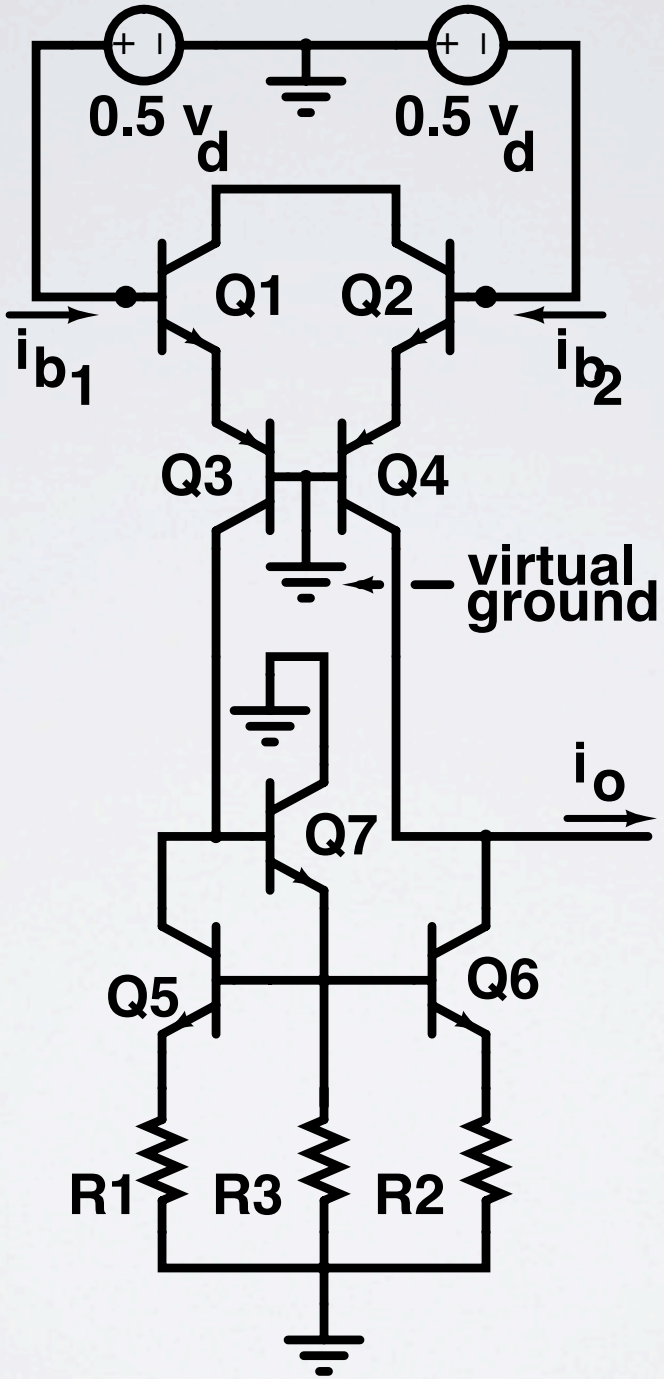
DC Quantities

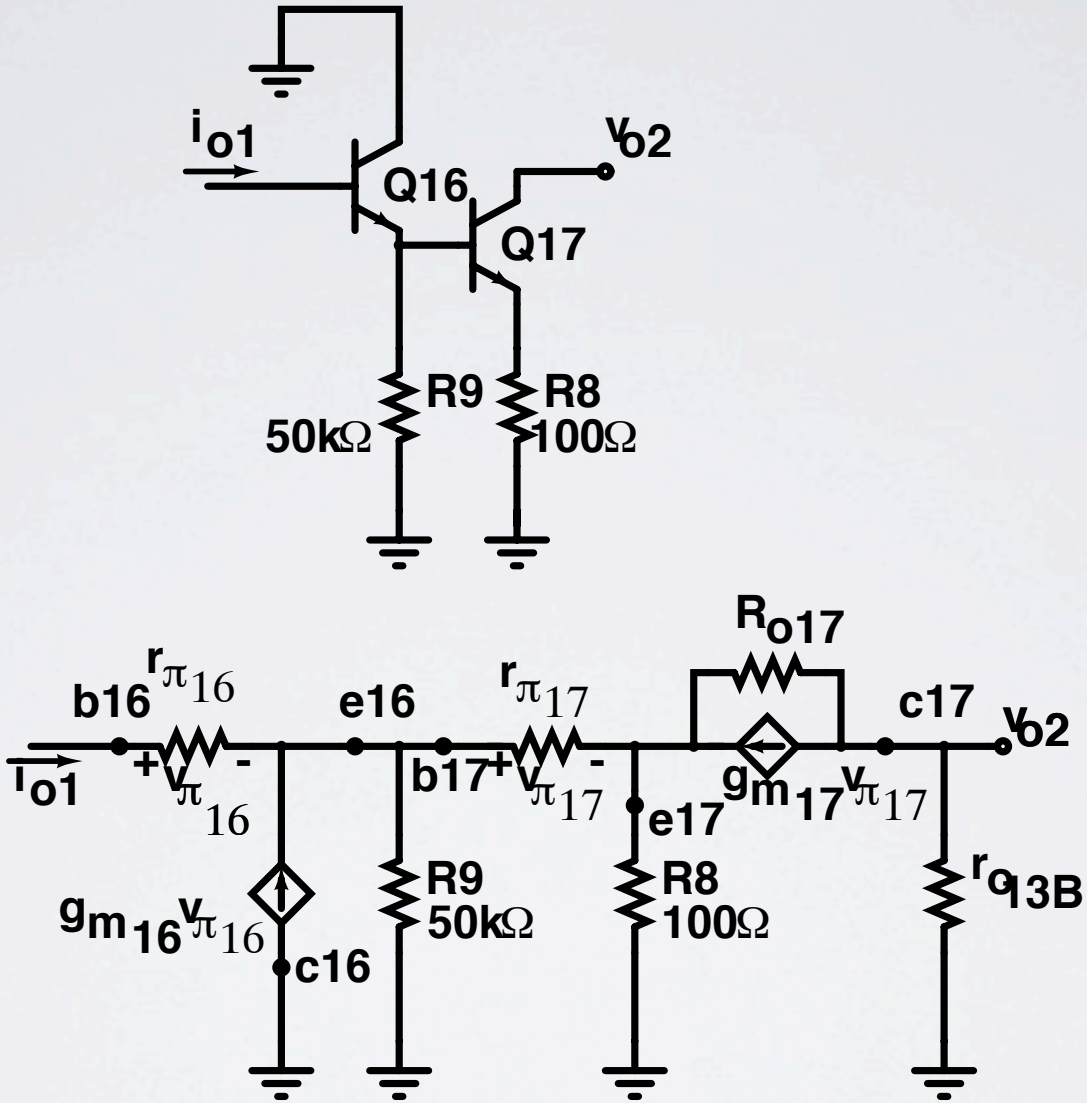
1. I_W
2. $I_{C,7}$
3. $I_{E,16}$
4. $V_{BE,19}$
5. Bias current
6. Offsets
7. CM input range

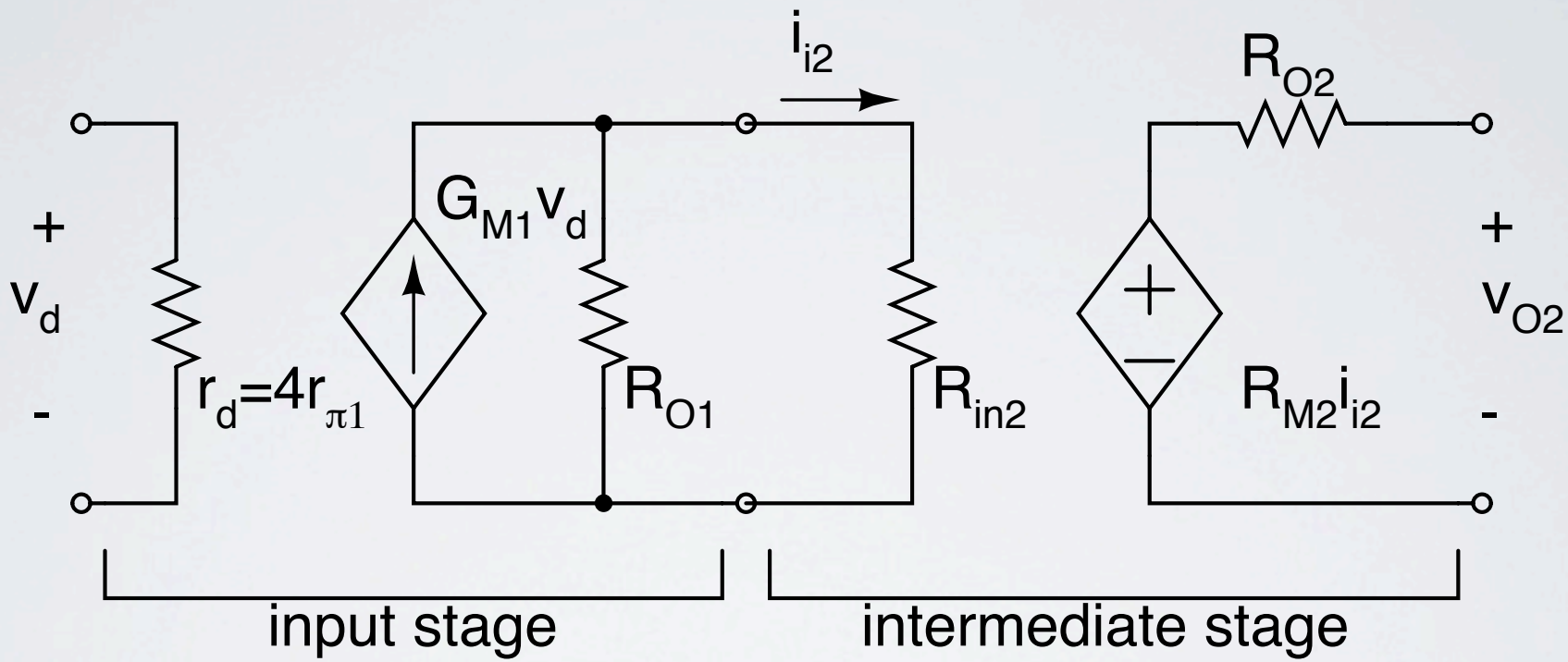
Textbook results for dc collector currents

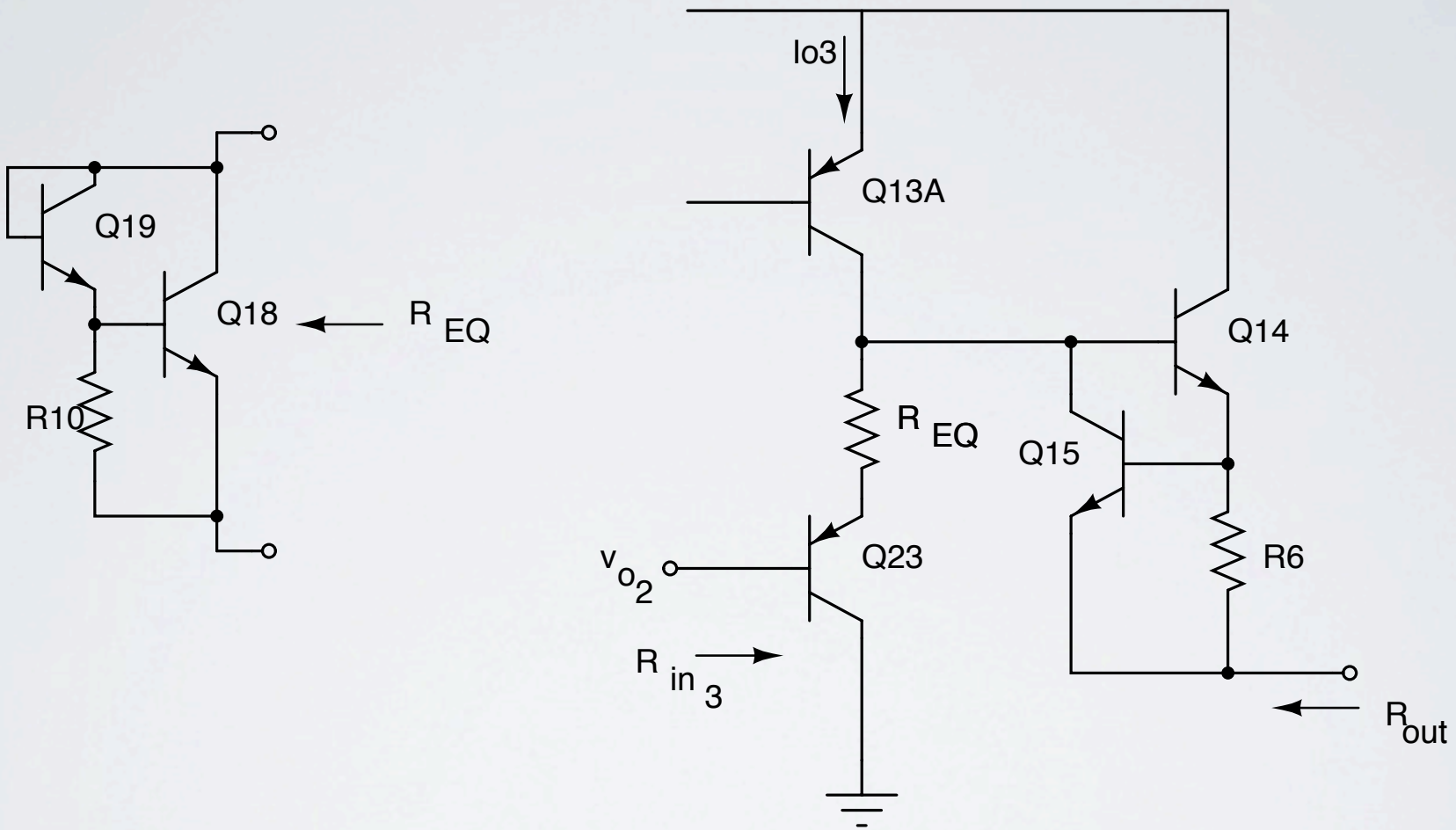
TABLE 9.1 Dc Collector Currents of the 741 Circuit (μA)

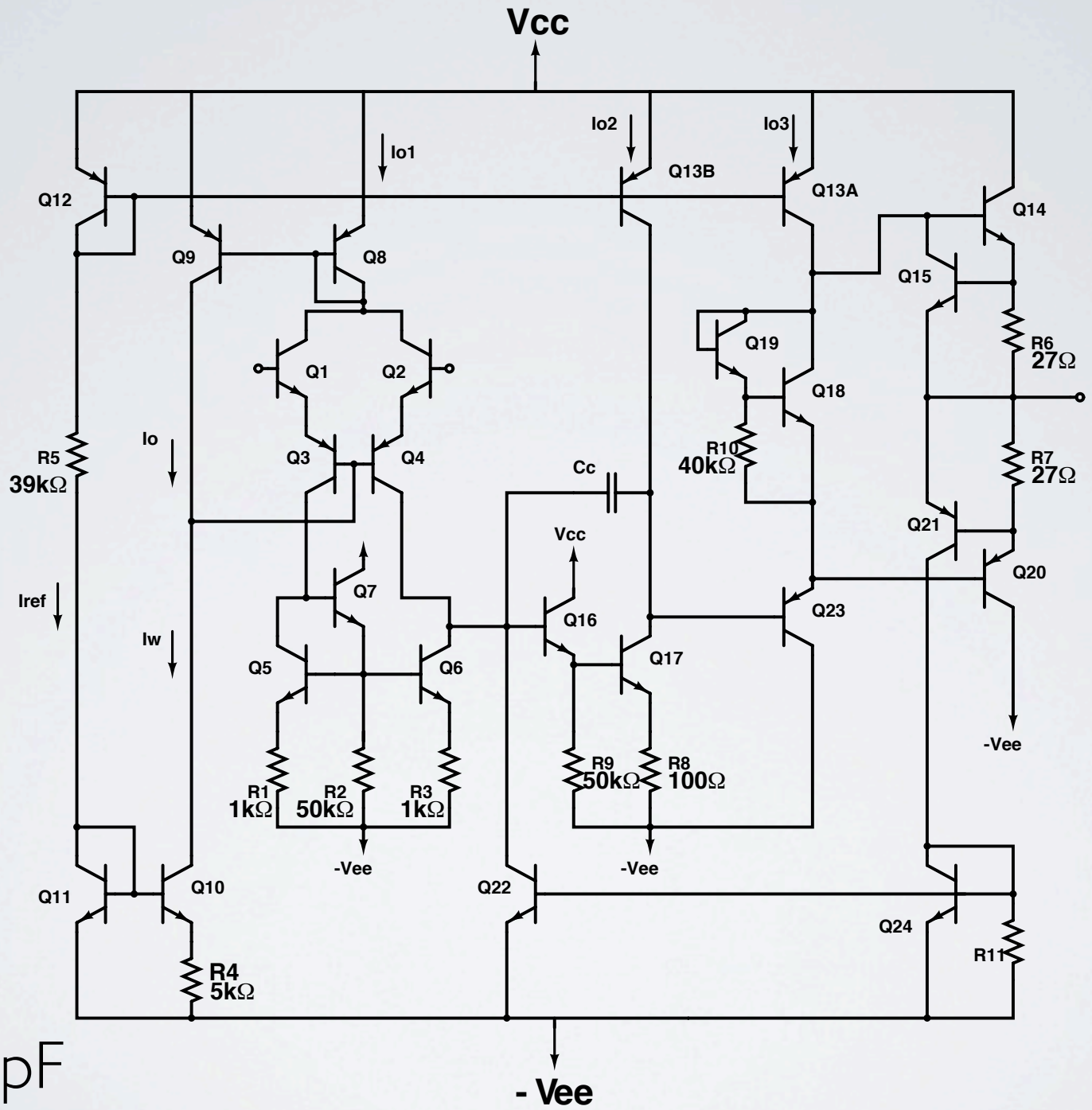
Q_1	9.5	Q_8	19	Q_{13B}	550	Q_{19}	15.8
Q_2	9.5	Q_9	19	Q_{14}	154	Q_{20}	154
Q_3	9.5	Q_{10}	19	Q_{15}	0	Q_{21}	0
Q_4	9.5	Q_{11}	730	Q_{16}	16.2	Q_{22}	0
Q_5	9.5	Q_{12}	730	Q_{17}	550	Q_{23}	180
Q_6	9.5	Q_{13A}	180	Q_{18}	165	Q_{24}	0
Q_7	10.5						


0.5 v_d
0.5 v_d
Q1
Q2
i_b1
i_b2
Q3
Q4
virtual ground
i_o
Q7
Q5
Q6
R1
R3
R2

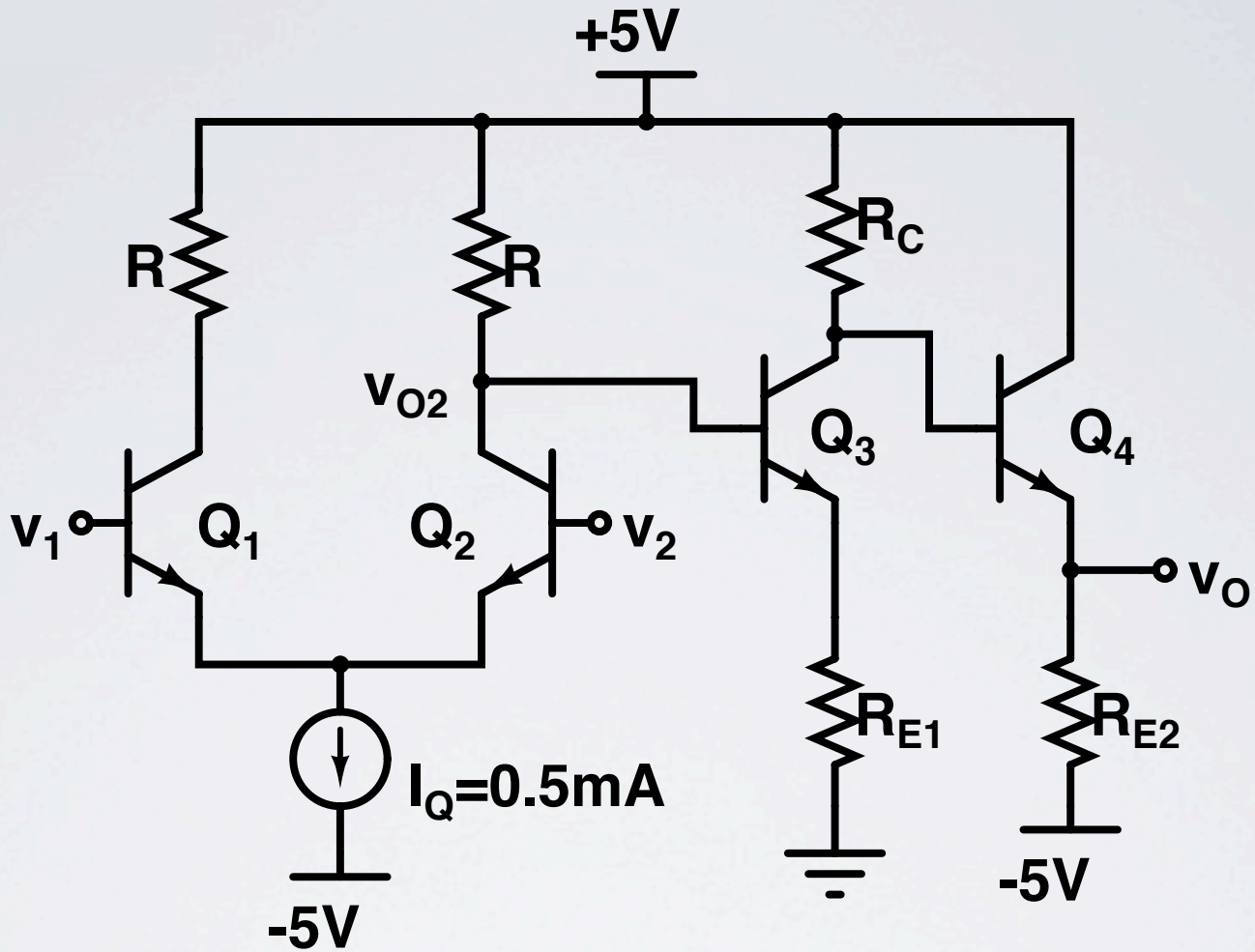

i o1
v o2
Q16
Q17
R9
50kΩ
R8
100Ω
R o17
r π16
r π17
b16
e16
c17
v o2
i o1
+ v π16 -
b17
+ v π17 -
g m17 v π17
e17
g m16 v π16
c16
R9
50kΩ
R8
100Ω
r o13B


i_{i2}
R_{O2}
+
v_d
-
$G_{M1}v_d$
$r_d=4r_{\pi 1}$
R_{O1}
R_{in2}
+
v_{O2}
-
$R_{M2}i_{i2}$
input stage
intermediate stage

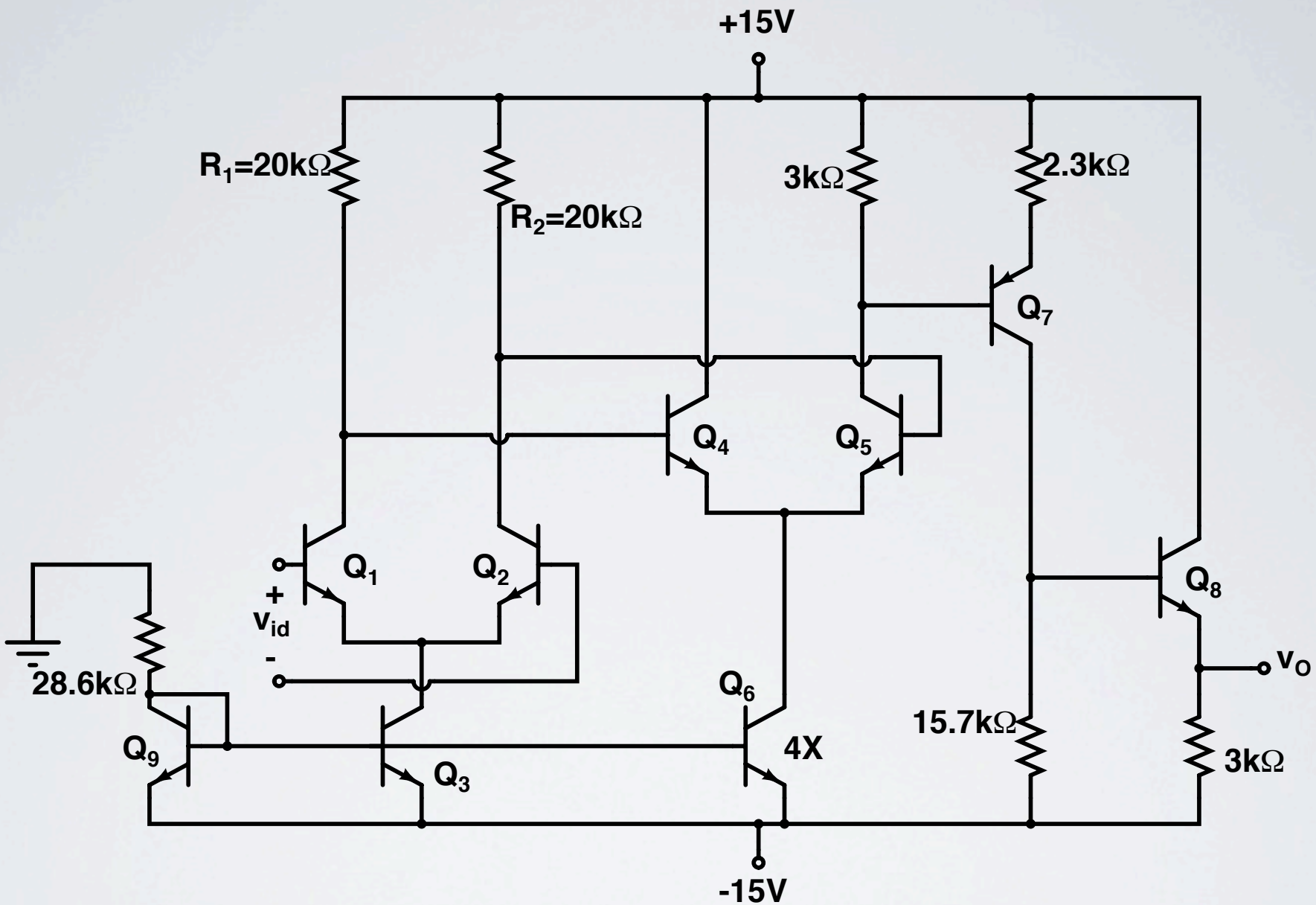

Q19
Q18
R EQ
R10
Io3
Q13A
Q14
R EQ
Q15
Q23
R6
v o2
R in 3
R out


Vcc
Io1
Io2
Io3
Q12
Q13B
Q13A
Q14
Q9
Q8
Q15
Q1
Q2
Q19
R6
27Ω
Q18
Io
R5
39kΩ
Q3
Q4
R10
40kΩ
Cc
R7
27Ω
Vcc
Q21
Iref
Q7
Q16
Q20
Q23
Iw
Q5
Q6
Q17
-Vee
R9
50kΩ
R8
100Ω
R1
1kΩ
R2
50kΩ
R3
1kΩ
-Vee
-Vee
Q11
Q10
Q22
Q24
R11
R4
5kΩ
- Vee

C_C=30pF



Assume h_{FE}=100, V_{BE}=0.7V, V_A=∞, $R_{O(CS)}$ =100kΩ (a) For v_1=v_2=0V, design so that v_{O2}=2V, v_{C3}=3V, I_{CQ3}=0.5mA, I_{CQ4}=3mA; (b) Find A_{d1}=v_{O2}/v_d & A_d=v_O/v_d; c) Find A_{cm1}=v_{o2}/v_{cm} and A_{cm}=v_O/v_{cm}, and the overall CMRR



Assume $h_{FE}=100, V_{BE(ON)}=0.7V$. Find: (a) (dc) I_C, V_C, V_E for al Q's, (b) Power dissipated at DC, (d) input bias current, (d) CM voltage range, (e) $A_d=v_O/v_{id}$