Operational Amplifiers

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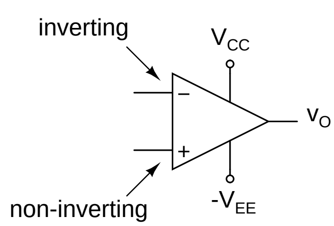
1 Introduction

The operational amplifier (*opamp* for short) is perhaps the most important building block for the design of analog circuits. Combined with simple negative feedback networks, opamps allow engineers to build many circuits in a simple fashion, at low cost and using relatively few discrete components. Good knowledge of the opamp characteristics and aplications is essencial for a sucessful analog engineer.

Opamps are *differential amplifiers*, and their output voltage is proportional to the difference of the two input voltages. The opamp's schematic symbol is shown below. The two input terminals, called the inverting and non-inverting, are labeled with - and +, respectively. Most opamps require two supplies that are most often connected to positive and negative voltages of equal magnitute. The supply connections may or may not be shown in a schematic diagram.



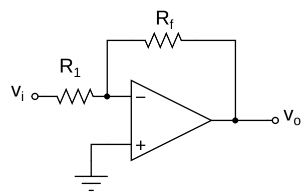
An ideal opamp has infinite gain and input impedance, and its input terminals take no input current. Negative feedback causes the voltage between inverting and non-inverting inputs to vanish. It is said that they are *virtually* connected. When one of the two inputs is connected to ground, the other one is said to be a *virtual ground*.

2 Basic Opamp Circuits

1. Inverting amplifier

   Since the opamp takes no input current, the same current flows through R_1 and R_2. Because the non-inverting input is grounded, a *virtual ground* exist in the inverting input by virtue of the infinite gain and the negative feedback being used. Thus $v_i = i \times R_1$ and $v_o = -i \times R_2$. It follows that the gain of the inverting amplifier is $\frac{v_o}{v_i} = -\frac{R_2}{R_1}$.

The input impedance $R_i = R_1$. To find the output impedance, apply a test current source to the output and ground to v_i. Because of virtual ground, no current flows through R_1. Since no current flows into the inverting input, the current through R_2 must be 0 as well. Thus, independently of the test current, v_o remains grounded in the ideal opamp. Consecuently the output resistance is ideally 0.



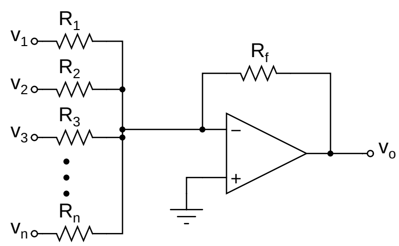
2. Summing amplifier

   A KCL at the inverting input yields

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + ... + \frac{v_n}{R_n} = -\frac{v_o}{R_f}$$

   Thus

$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + ... + \frac{R_f}{R_n}v_n\right)$$



3. Non-inverting amplifier

   Since the two opamp terminals must be at the same voltage,

$$i_1 = \frac{-v_i}{R_1}$$

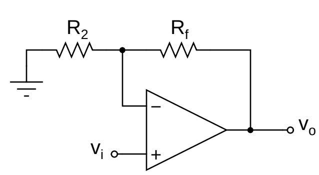
   and

$$i_2 = \frac{-v_i - v_o}{R_2}$$

   But no current flows into the inverting terminal, so $i_1 = i_2$. Substituting into this equation and solving for v_o yields

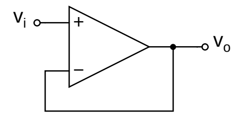
$$v_o = \left(1 + \frac{R_2}{R_1}\right) v_i$$

   Input impedance R_i is infinite. Output impedance is very low.



4. Voltage follower or *buffer* amplifier

   Since $R_f = 0$ and this configuration is the same than the non-inverting amplifier, the gain is unity. The input impedance is, however, infinity. So this configuration elliminates loading, allowing a source with a relatively large Thevenin's resistance to be connected to a load with a relatively small resistance.



5. Difference amplifier

   This circuit provides an output voltage that is proportional to the difference of the two inputs. Applying KCL at the inverting terminal yields

$$i_1 = \frac{v_1 - v_-}{R_1} = i_2 = \frac{v_- - v_o}{R_2}$$

   Solving for v_o and reordering terms gives

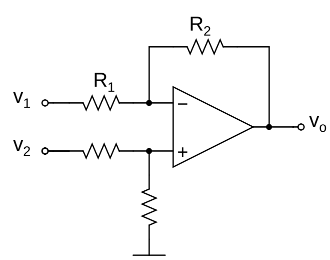
$$v_o = \frac{R_1 + R_2}{R_1} v_- - \frac{R_2}{R_1} v_1$$

   Since $v_- = v_+ = \frac{R_4}{R_3+R_4} v_2$,

$$v_o = \frac{R_1 + R_2}{R_1} \frac{R_4}{R_3 + R_4} v_2 - \frac{R_2}{R_1} v_1$$

   By choosing $R_1 = R_3$ and $R_2 = R_4$ one gets that

$$v_o = \frac{R_2}{R_1} (v_2 - v_1)$$



6. Current-to-voltage converter

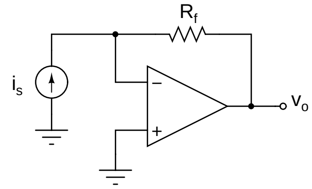
   Since the source current i_s can not flow into the amplifier's inverting input, it must flow thorugh R_f. Since the inverting input is virtual ground,

$$v_o = -i_s R_f$$

   Also, the virtual ground assumption implies that

$$R_i = 0$$

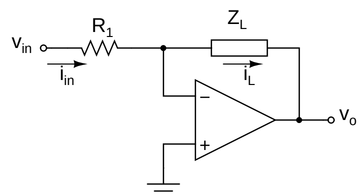
for this circuit.



7. Voltage-to-current converter

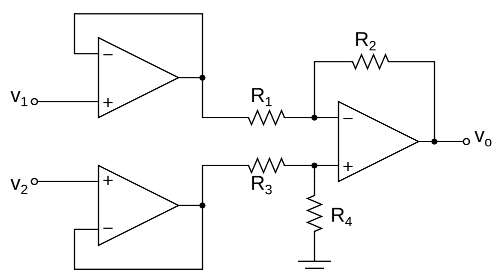
   In this cricuit, the load is not grounded but takes the place of the feedback resistor. Since the inverting input is virtual ground,

$$i_L = i_{in} = \frac{v_{in}}{R_1}$$



8. Instrumentation amplifier

   This amplifier is just two buffers followed by a differential amplifier. So it is a differential amplifier but the two sources see an infinite resistance load.



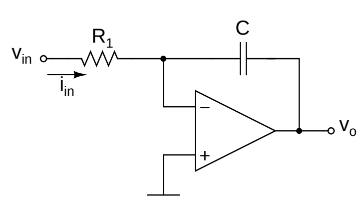
9. Integrator

   Let v_{in} be an arbitrary function of time. The current through the capacitor is $i_{in} = \frac{v_{in}}{R_1}$. From the capacitor law,

$$i_C = C\frac{dv_C}{dt}$$

   or

$$v_o = -v_C = -\frac{1}{C}\int i_C dt = -\frac{1}{R_1 C}\int v_{in} dt$$



10. Active low-pass filter

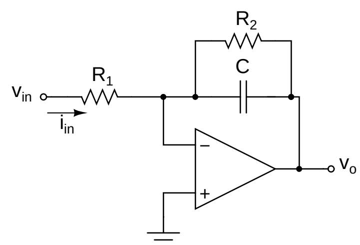
Here we assume that the input is sinusoidal. Thus we can use the concepts of impedance and reactance and work in the frequency domain. Thus, the circuit is an inverting amplifier, but the feedback resistor as been replaced with Z_f, the parallel combination of R_2 and C. Therefore,

$$Z_f = \frac{\frac{1}{sC}R_2}{\frac{1}{sC} + R_2} = \frac{R_2}{1 + sCR_2}$$

From the expression for the inverting amplifier's gain,

$$v_o(s) = -\frac{Z_f}{R_1} = -\frac{R_2}{R_1}\frac{1}{1 + sCR_2}v_i(s)$$

which is small for s large.



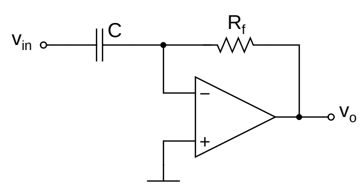
11. Differentiator

Here the input current is determined by the capacitor law,

$$i_{in} = C\frac{dv_{in}}{dt}$$

Thus

$$v_o = -R_f i_{in} = -R_f C\frac{dv_{in}}{dt}$$



12. Active high-pass filter

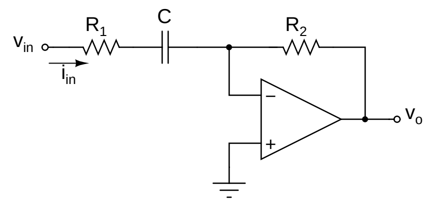
Like in the low-pass filter, we consider v_{in} to be sinusoidal and apply impedance concepts. The configuration is again like the inverting amplifier, but the resistor R_1 as been replaced with Z_1, which is R_1 in series with C. Thus

$$Z_1 = R_1 + \frac{1}{sC} = \frac{sR_1C + 1}{sC}$$

and

$$v_o = -\frac{R_f}{Z_1} = -\frac{sCR_f}{sR_1C + 1}$$

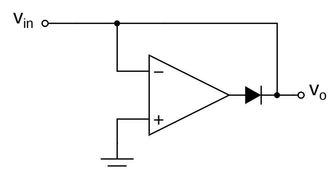
which is small for s small.



13. Precision half-wave rectifier

    In this circuit, the diode conducts when the opamp output is positive and larger than $0.7V$, i.e. when the non-inverting inputs exceeds the inverting by $\frac{0.7}{A_{open-loop}}$ volts, where $A_{open-loop}$ represents the opamp open-loop gain, taken to be infinity for an ideal device. Thus as soon as the input becomes negative, the diode conducts and the output becomes virtual ground. If the input is positive, the diode is an open circuit and the output is directly connected to the input.

    The circuit is used to rectify signals whose amplitude is smaller than the $0.7V$ required to forward-bias the diode.



14. logarithmic amplifier

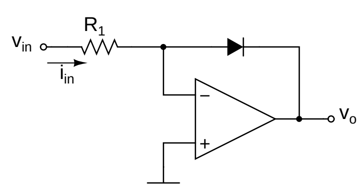
    Here output and diode's voltage are equal in magnitude and of opposite signs. Since

$$i_D \approx I_S exp\left(\frac{v_D}{V_T}\right)$$

    where V_T is the thermal voltage, equal to $25mV$ at room temperature. It follows that

$$v_o = -v_D = -V_T\left(log(v_{in}/R_1) - logI_s\right)$$

    and is thus proportional to the logarithm off the input.



15. Antilogarithmic amplifier

    The current i_{IN} is given by

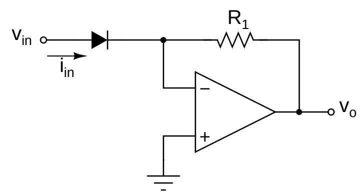
$$i_D \approx I_S exp\left(\frac{v_D}{V_T}\right)$$

    or

$$i_{IN} \approx I_S exp\left(\frac{v_{IN}}{V_T}\right)$$

Thus the output voltage is

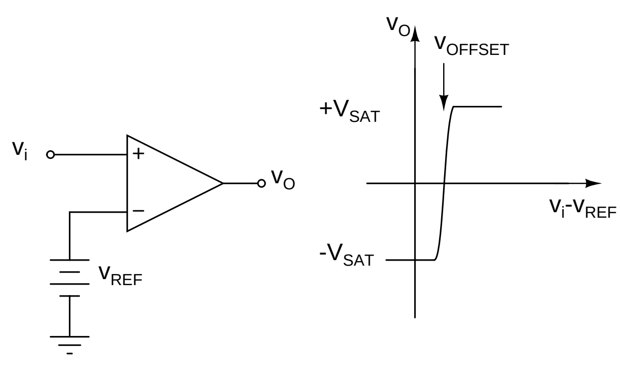
$$v_O = -i_{IN}R_f \approx I_S R_f exp\left(\frac{v_{IN}}{V_T}\right)$$



16. Comparator

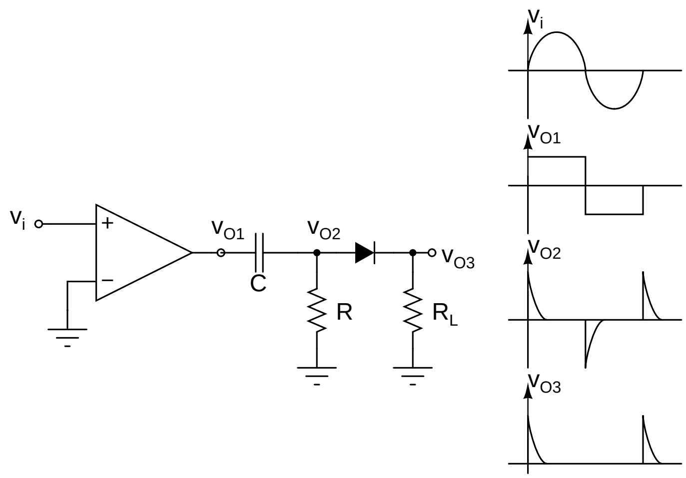
An opamp can be used as a comparator in a circuit like the one shown below. This is a non-linear circuit in which the output saturates to about 90 % of the positive and negative supply voltages. The polarity of the output voltage depends on the sign of the differential input, $v_i - v_{REF}$.

The sketch shows non-ideal characteristics tipically found in opamps. The offset voltage, v_{OFFSET}, is on the order of few millivolts and causes the transition from low to high to be slightly displaced from the origin. v_{OFFSET} can be negative or positive, and is zero in an ideal opamp. The posibility of having voltages between plus and minus v_{SAT}, a consecuense of the finite gain of practical opamps, is also shown. This part of the curve would be vertical if the opamp is ideal. Special integrated circuits (like the MC1530) are specially build to be used as comparators and minimize these non-ideal effects.



17. Zero-crossing detector

If the inverting input of a comparator is connected to ground, the device's output switches from positive to negative saturation when the input goes from positive to negative, and viceversa. Output v_{O1} on the following sketch displays this vehavior.

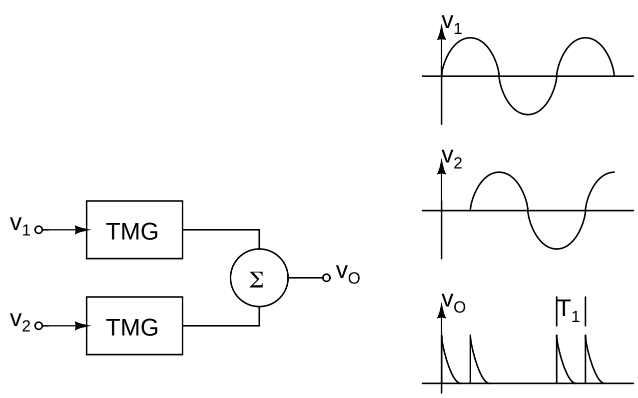


18. Timing-marker generator

    If an RC network is connected to the output of a zero-crossing detector, capacitor charging and discharging produce the waveform v_{O2} shown in the above sketch. This signal is rectified to produce the waveform labeled v_{O3}. The circuit is called a *timing-markers generator*, or TMG, for obvious reasons.

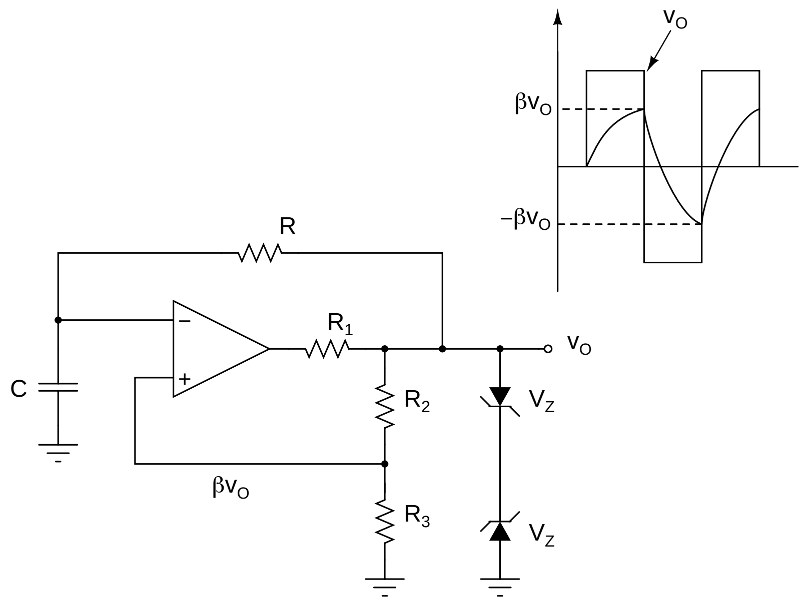
19. Phase meter

    Combining two TMG and an adder, as shown in the following figure, one can build the so called *phase meter*. The time difference T_1 is proportional to the phase difference between the two sinusoidal inputs.



20. Square Wave Generator

    This circuit is an oscillator that generates a square wave. It is also known as an *astable multivibrator*. The opamp works as a comparator. Let's assume that the opamp output goes high on power-on, thus making $v_O = +V_Z$. The capacitor charges with a time constant $\tau = RC$. When the capacitor voltage reaches $\beta v_O = \frac{R_3}{R_2+R_3}$, the opamp output switches low, and $v_O = -V_Z$ as shown in the graph.

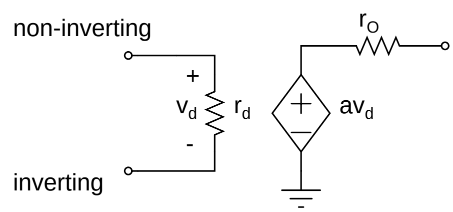


R
R_1
R_2
R_3
C
V_Z
V_Z
v_O
βv_O
v_O
βv_O
$-\beta v_O$

3 Limitations and Second Order Effects on Real Opamps

1 Gain, Input and Output Resistance

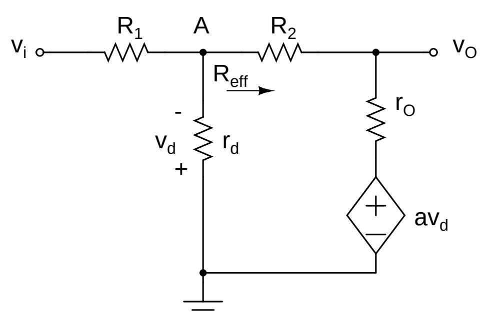
Real operational amplifiers have finite input resistance and gain, as well as non-zero output resistance. We can represent the opamp by its two-port equivalent network, shown below. Analysis of circuits consist on replacing the opamp by its two-port equivalent and performing network analysis.



1.1 Inverting Amplifier

Voltage Gain

After replacing the opamp by its equivalent circuit, the schematic diagram of the inverting amplifier looks as follows.



We can write the two node equations and solve them simultaneously to obtain the voltage gain. However, the algebra becomes simpler if we invoke the voltage divider rule to express the voltage v_d in terms of the output voltage. This yields

$$v_O = av_d + (-v_d - av_d)\frac{r_O}{R_2 + r_O}$$

After rearranging, this gives

$$v_d = \frac{v_O}{a - (1+a)\frac{r_O}{r_O+R_2}}$$

Since a is always very large, we can approximate $1 + a$ as a. This gives

$$v_d = v_O/\alpha \tag{1}$$

where

$$\alpha = \frac{aR_2}{r_O + R_2}$$

We can now apply KCL to the node between R_1 and R_2 to get

$$\frac{v_i + v_O/\alpha}{R_1} = -\frac{v_O/\alpha}{r_d} - \frac{v_O/\alpha + v_O}{R_2}$$

Multiplying the whole expression by αR_2 gives

$$\alpha\frac{R_2}{R_1}v_i + \frac{R_2}{R_1}v_O = -\left(\frac{R_2}{r_d} + \alpha + 1\right) v_O$$

After rearrangement,

$$A_v = \frac{v_O}{v_i} = -\frac{R_2}{R_1}\frac{\alpha}{1 + \alpha + \frac{R_2}{r_d||R_1}}$$

A well designed inverting amplifier will use $R_2 >> r_O$ to avoid excesive loading at the output, and $R_1 << r_d$ to avoid excesive loading at the input. Under these conditions,

$$A_v = \frac{v_O}{v_i} = -\frac{R_2}{R_1}\frac{a}{1 + a + \frac{R_2}{R_1}}$$

Input Resistance

By inspection of the circuit diagram,

$$R_{in} = R_1 + r_d||R_{eff}$$

where R_{eff} is the effective resisitance seen when looking from point A towards the right, as shown in the diagram. Applying a test source v_A at point A and observing that $v_A = -v_d$,

$$i_A = \frac{v_A + av_A}{R_2 + r_O}$$

so

$$R_{eff} = \frac{v_A}{i_A} = \frac{r_O + R_2}{1 + a}$$

The input resistance then becomes

$$R_{in} = R_1 + r_d||\frac{r_O + R_2}{1 + a}$$

Assuming a well design amplifier,

$$R_{in} = R_1 + \frac{R_2}{1 + a}$$

Output Resistance

Grounding the input and applying a test source v_{TEST} to the output terminal yields a test current given by

$$i_{TEST} = \frac{v_{TEST}}{R_{eq}} + \frac{v_{TEST} - av_d}{r_O}$$

where

$$R_{eq} = R_2 + R_1||r_d$$

Applying the voltage divider rule

$$v_d = -\frac{R_1||r_d}{R_{eq}} v_{TEST}$$

which yields

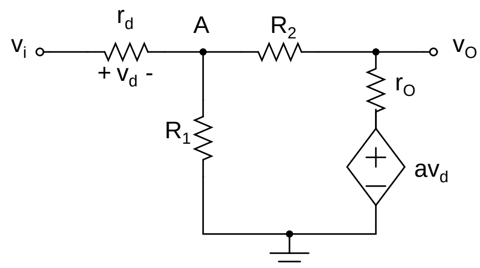
$$R_{OUT} = \frac{v_{TEST}}{i_{TEST}} = R_{eq}||\frac{r_O}{1 + a\frac{R_1||r_d}{R_{eq}}}$$

For a well designed amplifier

$$R_{OUT} = \frac{r_O}{1 + a\frac{R_1}{R_1+R_2}}$$

1.2 Non-inverting Amplifier

After replacing the opamp by its equivalent circuit, the schematic diagram of the non-inverting amplifier looks as follows.



Applying the voltage divider rule to express the output voltage in terms of the voltage at point A, v_A, yields

$$v_O = \frac{v_A - av_d}{R_2 + r_O} r_O + av_d$$

To elliminate v_A, express it as $v_i - v_d$ tp obtain

$$v_O = \frac{v_i - v_d - av_d}{R_2 + r_O} r_O + av_d$$

which, after combining the two terms on the right hand side, cancelling common terms with opposite signs and rearranging, gives

$$v_O = \frac{r_O}{R_2 + r_O} v_i + \frac{aR_2 - r_O}{R_2 + r_O} v_d$$

Solving for v_D yields

$$v_d = b_1 v_O - b_2 v_i = \frac{R_2 + r_O}{aR_2 - r_O} v_O - \frac{r_O}{aR_2 - r_O} v_i$$

where b_1 and b_2 are defined in the equation. To simplify this expression further, let's invoke the "good design rule" previously established: to avoid output loading, select $R_2 >> r_O$. Assuming that the rule is followed,

$$v_d \approx \frac{1}{a} v_O - \frac{1}{a}\frac{r_O}{R_2} v_i$$

Since for amplifiers ussually $v_i < v_O$, the second term can be neglected and

$$v_d \approx v_O/a$$

Applying KCL at node A and replacing v_d for $\frac{v_O}{a}$ yield

$$\frac{v_O/a}{r_d} = \frac{v_i - v_O/a}{R_1} + \frac{v_i - v_O/a - v_O}{R_2}$$

Multiplying the whole expression by aR_2 gives

$$\frac{R_2}{r_d}v_O = \frac{R_2}{R_1}av_i - \frac{R_2}{R_1}v_O + av_i - v_O - av_O$$

which, after rearrangement, becomes

$$A_v = \frac{v_O}{v_i} = \left(1 + \frac{R_2}{R_1}\right)\frac{a}{1 + a + \frac{R_2}{r_d||R_1}}$$

Input Resistance

Applying a test source at the input and applying KCL at node A gives

$$i_{TEST} = \frac{v_d}{r_d} = \frac{v_i - v_d}{R_1} + \frac{v_i - v_d - av_d}{R_2}$$

where r_O as been neglected. Solving for v_d gives

$$v_d = \frac{r_d||R_1||\frac{R_2}{a+1}}{R_1||R_2}v_i$$

Thus,

$$i_i = \frac{r_d||R_1||\frac{R_2}{a+1}}{r_d(R_1||R_2)}v_i$$

and

$$R_{in} = \frac{v_i}{i_i} = r_d\frac{R_1||R_2}{r_d||R_1||\frac{R_2}{a+1}}$$

Since for any practical design $R_2 << aR_1$, and assuming that for a good design R_1 is selected much smaller that r_d,

$$R_{in} \approx ar_d\frac{R_1}{R_1 + R_2} = ar_d\frac{1}{1 + \frac{R_2}{R_1}} = r_d\frac{a}{A_{v,ideal}}$$

where $A_{v,ideal}$ is the expected voltage gain for the non-inverting amplifier. Thus, it can be safely assumed that the input resistance will be a few orders of magnitude larger than r_d, an already large resistance.

Output Resistance

Inspection of the circuit diagrams for the inverting and non-inverting amplifiers after the input node is grounded reveals that there is no difference between the two. Thus, our results for the inverting amplifier's output resistance apply to the non-inverting amplifier without modification.

2 Input Bias and Offset Current

Non-ideal amplifier biasing requires a small amount of current to flow into the input terminals. Due to unavoidable imperfections in the manufacturing process, the currents that flow into the inputs, I_n and I_p, are not exactly equal. This gives place to two parameters, called *bias* and *offset* currents, normally specified in the opamp data sheets. The bias current is defined as the average current flowing into the inputs.

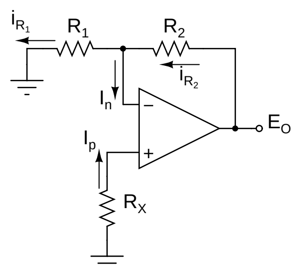
$$I_B = I_p + I_n$$

The offset currents is absolute value of the difference between the two input currents.

$$I_{OS} = |I_p - I_n|$$

The sense of I_B is determined by the type of transistor used in the device's input stage, entering and exiting for NPN and PNP input transistors, respectively. The offset current sign can not be predicted and changes from device to device. The offset current is typically an order of magnitude smaller that the bias current.

To get an idea of the importance the bias current can have in the operation of a circuit, consider the following diagram.



By considering the bias currents with grounded inputs, we can find out the output error due to the currents. Proper selection of resistor R_x will allow us to partially cancel out such error, as we will see. We assume that, in spite of the presence of the bias currents, the two input terminals are virtually connected. Thus, from Ohm's law,

$$v_n = v_p = -I_p R_x$$

and

$$i_{R_1} = -\frac{R_x}{R_1} I_p$$

The output error is then given by

$$E_O = -I_p R_x + (I_n - \frac{R_x}{R_1} I_p) R_2$$

If, for example, we neglect the offset current and assume that $I_p = I_n = 80nA$, $R_x = 0$, $R_1 = 22k\Omega$ and $R_2 = 2.2M\Omega$, the output error is $2.2 \times 10^6 \times 80 \times 10^{-9} = .176V$, a quantity unaceptable for many applications. We can see, however, that by reducing the size of R_2 the error can be reduced. Also, if we select

$$R_x = R_1 || R_2$$

we can completely cancel out the error due to I_B, and be left out with smaller error due to I_{OS}. For further reductions we can select an amplifier with smaller values of I_B and I_{OS}, or trim the error down manually.

3 Input Offset Voltage

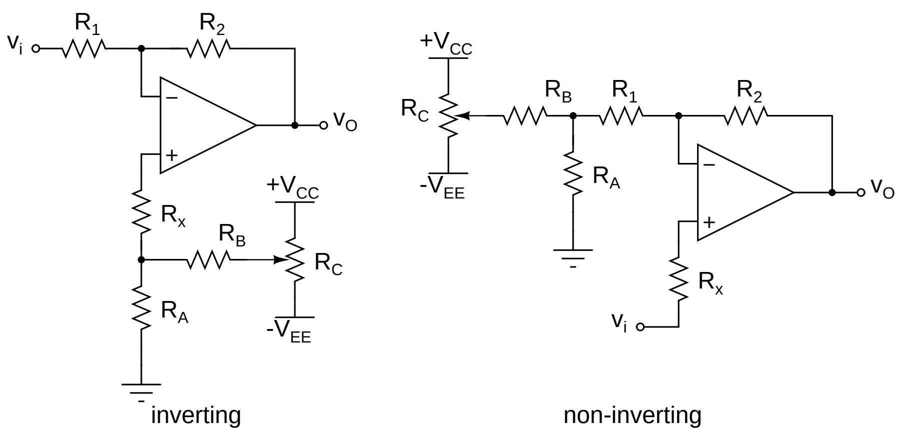
If the two inputs of an opamp are connected together, ideally the output voltage should be zero. An actual opamp, due to unavoidable fabrication errors, will yield a non-zero output even if the inputs are tied together. To make the output zero, a suitable correcting voltage must be applied at the input. This voltage is called the *input offset voltage* and is represented by V_{OS}.

The polarity of V_{OS} is not known in advance. A value of $1mV$ is typical, with something like $5mV$ being the maximum. This voltage is amplified with the same gain than the input signal, and can thus lead to a large output error. If the amplifier's gain is, for instance, 1000, the output error can be up to $\pm 5V$!

4 Offset Nulling

The reduction of errors due to both V_{OS} and I_{OS} can be achieved by applying an external dc input voltage such that the output voltage is made zero when no input is present. The required voltage can be obtained from the supplies using a voltage divider network. The correction must be adjusted once the circuit is assembled by means of adjusting a potentiometer.

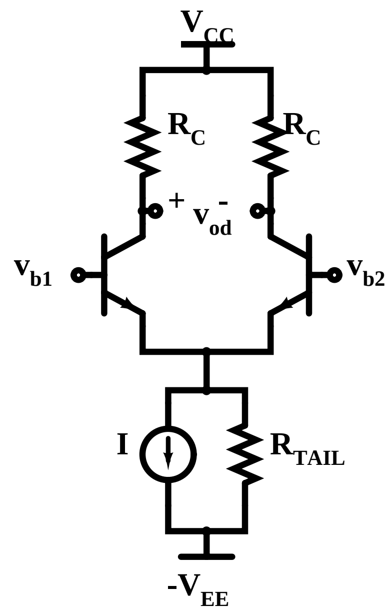
Setups that can be used for offset nulling are shown below for both inverting and non-inverting amplifiers. Resistor values must be selected to make possible to correct for the largest possible offset. It is a good practice to select $R_B < R_C$ to avoid loading the potentiometer's voltage divider. For the inverting amplifier, R_A should be much smaller that R_x to avoid altering the resistance levels. Likewise, $R_A << R_1$ to avoid altering the gain of the non-inverting amplifier. If this is not feasible, R_1 should be decreased to incorporate R_A and still have the same gain.



Offset Nulling Networks

4 Differential Amplifiers

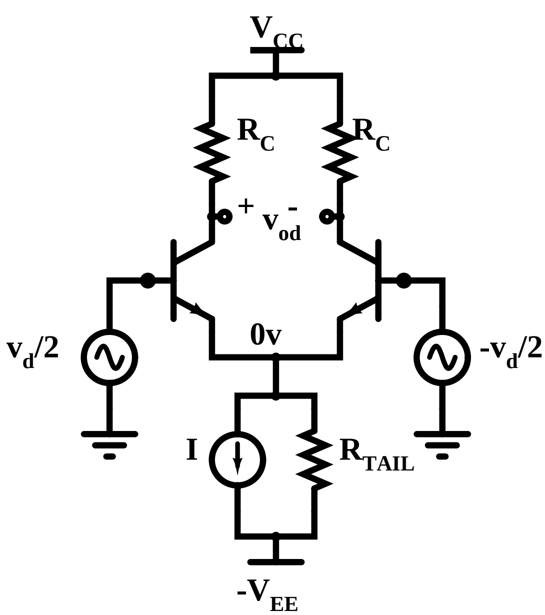
Differential Stage

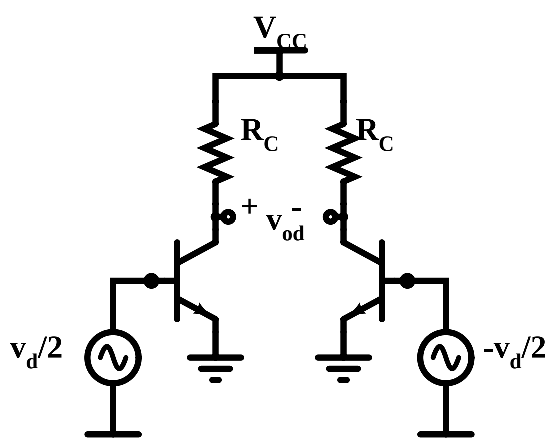


$$v_{b1} = v_{CM} + \frac{v_d}{2}; v_{b2} = v_{CM} - \frac{v_d}{2}$$

Superposicion: consider
differential mode $\rightarrow \pm\frac{v_d}{2}$
common mode $\rightarrow v_{CM}$

Differential mode

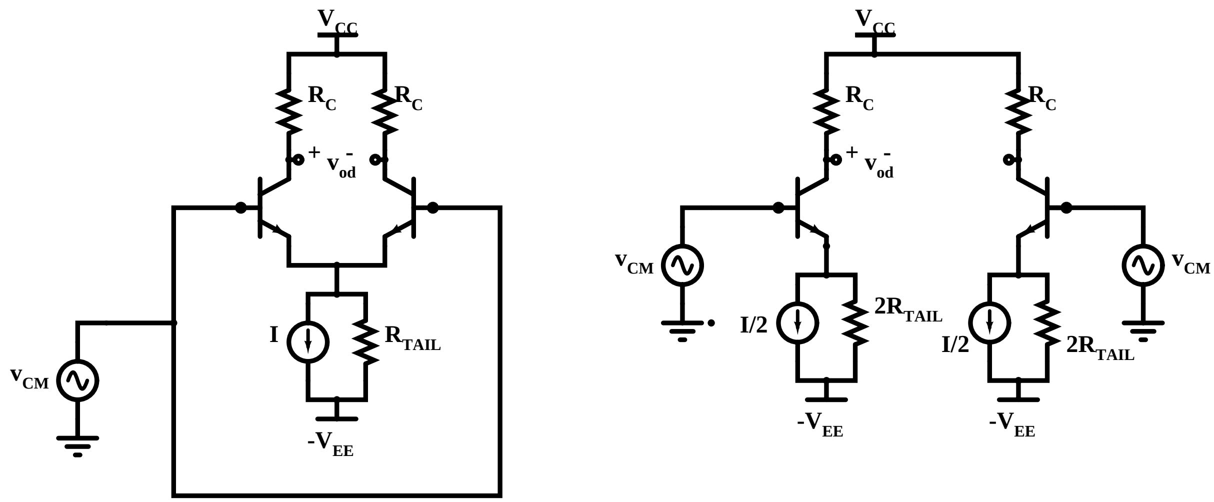




$$A_d = -g_m R_C$$

$$R_{id} = 2r_\pi$$

Common mode



$$\begin{aligned} A_{CM} &= \frac{v_{c1}}{v_{CM}} = -\frac{\beta R_C}{r_\pi + (\beta+1)2R_{TAIL}} \\ &\approx -\frac{g_m R_C}{1 + g_m 2R_{TAIL}} \end{aligned}$$

$$CMRR = \mid \frac{A_d}{A_{CM}} \mid = \frac{1}{2}(1 + 2g_m R_{TAIL})$$

where $A_d = \frac{v_{c1}}{v_d} = -\frac{1}{2}g_m R_C$.
Common mode input resistance:

$$R_{i_{CM}} = r_\pi + (\beta+1)2R_{TAIL}$$

Input Offset Voltage

Due to fabrication errors, even if we connect the two transistor bases to ground, $v_o \neq 0$. The *input offset voltage* is defined as

$$v_{OS} = \frac{v_o}{A_d}$$

Example: $R_{C1} = R_C + \frac{\Delta R_C}{2}$, $R_{C2} = R_C - \frac{\Delta R_C}{2}$

$$v_{C1} = V_{CC} - \alpha\frac{I}{2}(R_C + \frac{\Delta R_C}{2})$$

$$v_{C2} = V_{CC} - \alpha\frac{I}{2}(R_C - \frac{\Delta R_C}{2})$$

$$v_o = v_{C1} - v_{C2} = -\alpha \frac{I}{2} \Delta R_C$$

Using $A_d = -g_m R_C = -\alpha \frac{I/2}{V_T} R_C$

$$v_{OS} = V_T \frac{\Delta R_C}{R_C}$$

Input Bias and Offset Currents

If perfectly symmetric

$$I_B = I_{B1} = I_{B2} = \frac{I/2}{\beta + 1}$$

Offset current: $I_{B1} \neq I_{B2}$, $I_{OS} \equiv\mid I_{B1} - I_{B2} \mid$
Example: $\beta_1 = \beta + \frac{\Delta\beta}{2}$, $\beta_2 = \beta - \frac{\Delta\beta}{2}$

$$I_{B1} = \frac{I/2}{\beta + \frac{\Delta\beta}{2} + 1}$$

$$I_{B2} = \frac{I/2}{\beta - \frac{\Delta\beta}{2} + 1}$$

Let

$$\frac{1}{\beta + 1 \pm \frac{\Delta\beta}{2}} \approx \frac{1}{\beta + 1} \left(1 \mp \frac{\Delta\beta}{2\beta}\right)$$

Then

$$I_{OS} = \frac{I}{2(\beta + 1)} \frac{\Delta\beta}{\beta} = I_B \frac{\Delta\beta}{\beta}$$

5 Current Sources

Generally, analog integrated circuits use current sources for biasing. Because their large output resistance, current sources allow the design of amplifiers with low sensitivity and high gain. This is difficult to obtain from configurations that use resistors to set the operating point because low sensitivity requires the use of an un-bypassed emitter resistor that would also reduce the amplifier's gain.

Some transistor circuits used to implement current sources are shown in figure 1 In the remaining of this section, these circuits are analyzed. Notice that transistors with matched properties are required for proper operation in all these circuits.

1 Basic Configuration

The simplest current source is also known as a current mirror. It works because the two transistors are matched and share the same base-to-emitter voltage, and therefore their collector currents must be identical.

If we neglect the base currents, the collector current of Q_1 (the reference transitor) is approximately equal to *reference* current. Transistor Q_2 *mirrors* the collector current of Q_1, and thus

$$I_o = I_{C1} = I_{ref} - 2 \times I_B = I_{ref} - \frac{2 \times I_{C1}}{\beta}$$

where I_{C1} and I_{C2} refer to the collector currents of Q_1 and Q_2. After rearranging, we get that

$$I_o = \frac{\beta}{\beta+2} I_{ref}$$

We can scale the collector cuurents by an arbitrary factor by fabricating the transistor with different areas. The ratio of the areas is also the scale factor. Thus,

$$I_o = \frac{A_{Q2}}{A_{Q1}} \frac{\beta}{\beta+2} I_{ref}$$

where A_{Q2} and A_{Q1} stand for mirror and reference transistor areas, respectively.

In hand analysis it is usual to consider β large, approximate the base-to-emitter voltage to $0.7V$, and neglect the two base currents. Thus

$$I_o \approx \frac{A_m}{A_{ref}} \frac{V_{CC} + V_{EE} - 0.7}{R}$$

2 Current Source with Base-current Compensation

By adding a third transistor to buffer the two base currents, reference transistor's collector and reference currents become related by

$$I_{C1} = I_{ref} - \frac{2I_B}{\beta+1}$$

replacing I_B for $\frac{I_{C1}}{\beta}$, setting $I_o = I_{C1}$ and rearranging yields

$$I_o = \frac{\beta^2+\beta}{\beta^2+\beta+2} I_{ref}$$

3 Wilson Current Source

Q_3's emitter transistor current is

$$I_{E3} = \frac{\beta+1}{\beta} I_o = 2I_B + I_{C2}$$

Setting $I_B = \frac{I_{C1}}{\beta}$ and $I_{C2} = I_{C1}$ gives

$$\frac{\beta+1}{\beta} I_o = \frac{\beta+2}{\beta} I_{C1}$$

The reference transistor collector current is given by

$$I_{C1} = I_{ref} - \frac{I_o}{\beta}$$

Combining the last two expressions and rearranging give

$$I_o = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} I_{ref}$$

where

$$I_{ref} \approx \frac{V_{CC} + V_{EE} - 1.4V}{R}$$

4 Source with Emitter Resistors

Applying KVL on the bottom loop gives, after rearranging

$$I_o \approx \frac{V_{BE_1} - V_{BE_2} + I_{ref}R_1}{R_2}$$

which, assuming equal base-emitter voltages, gives

$$I_o \approx \frac{R_1}{R_2} I_{ref}$$

with

$$I_{ref} \approx \frac{V_{CC} + V_{EE} - 0.7V}{R_1 + R}$$

5 Widlar Source

Applying KVL on the left branch gives

$$I_{ref} = \frac{V_{CC} + V_{EE} - 0.7V}{R}$$

In the bottom loop, KVL yields

$$V_{BE_2} = V_{BE_1} - \frac{\beta + 1}{\beta} I_o R_M$$

The base-to-emitter voltages can be expressed in terms of the currents

$$V_{BE_1} = V_T ln(\frac{I_{C1}}{I_S}) = V_T ln(I_{C1}) - V_T ln(I_S)$$

where I_S is the reverse saturation current, a transistor parameter. Similarly

$$V_{BE_2} = V_T ln(\frac{I_o}{I_S}) = V_T ln(I_o) - V_T ln(I_S)$$

Thus

$$V_T ln(I_o) = V_T ln(I_{C1}) - \frac{\beta + 1}{\beta} I_o R_M$$

which after setting $\frac{\beta+1}{\beta} \approx 1$, yields

$$I_o = \frac{V_T}{R_M} ln(\frac{I_{C1}}{I_o})$$

which can be solved iteratively to obtain I_o.

6 Output Resistance of Current Sources

Ideal current sources have infinite output resistance. The above circuits will approximate an ideal current source as long as the mirror transistor works in the active region. To estimate their output resistances in a more or less general way[1], we will consider the mirror with emitter resistors, shown in figure 2.

The equivalent circuit is shown in the right side of the figure.

Since the voltage accross Q1's dependant current source is v_{π_1}, the source is equivalent to a resistor of value $\frac{1}{g_{m_1}}$. Thus the Q1 side of the circuit can be replaced by its Thevenin resistance

$$R_{TH} = \frac{1}{g_{m_1}} \parallel r_{\pi_1} + R_1$$

Replacing $g_{m_1} = \frac{r_{\pi_1}}{\beta}$ gives

$$R_{TH} = \frac{r_{\pi_1}}{\beta + 1} + R_1$$

Our objective is to find the output resistance, so we will apply a test voltage source to the output node and replace the independent current source with an open circuit. The resulting circuit is shown in figure 3.

Applying KVL to the right hand side loop gives

$$v_{TEST} = (i_{TEST} - g_{m_2} v_{\pi_2}) r_o + i_{TEST} \left((r_{\pi_2} + R_{TH}) \parallel R_2 \right) \tag{2}$$

To find v_{π_2} in terms of i_{TEST}, find the voltage at node A and apply the voltage divider rule. This yields

$$v_{\pi_2} = -i_{TEST} \left((R_{TH} + r_{\pi_2}) \parallel R_2 \right) \frac{r_{\pi_2}}{R_{TH} + r_{\pi_2}}$$

which after some algebra gives

$$v_{\pi_2} = -i_{TEST} \frac{r_{\pi_2} R_2}{R_{TH} + r_{\pi_2} + R_2}$$

Substituting into equation 1 and simplifying yields

$$R_{OUT} = \frac{v_{TEST}}{i_{TEST}} = r_o \left(1 + \frac{\beta R_2}{R_{TH} + r_{\pi_2} + R_2} \right) + R_P \approx r_o \left(1 + \frac{\beta R_2}{R_{TH} + r_{\pi_2} + R_2} \right) \tag{3}$$

where

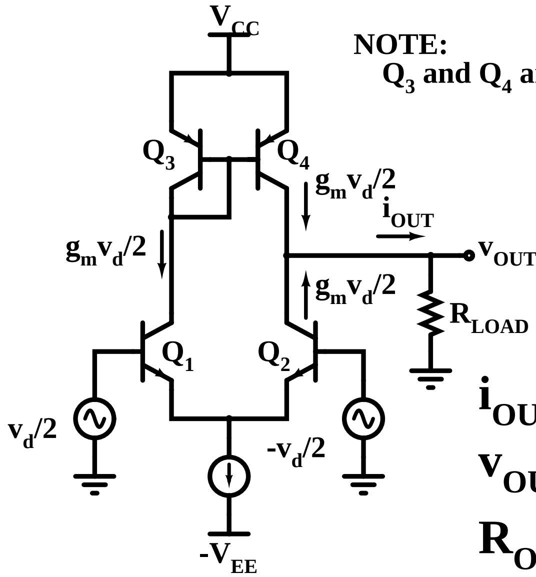
$$R_P = (R_{TH} + r_{\pi_2}) \parallel R_2$$

For the Midlar mirror, $R_1 = 0$ and $R_{TH} \approx \frac{r_{\pi_1}}{\beta+1} \ll r_{\pi_2} + R_2$. If r_{π_2} is also much larger that R_2, then

$$R_{OUT} \simeq r_o \left(1 + g_{m_2} R_2 \right)$$

[1]Indeed, you can apply the results of this section to any circuit consisting of a transistor with resistors R_{TH} and R_2 at base and emitter, respectively.

6 Active Loads

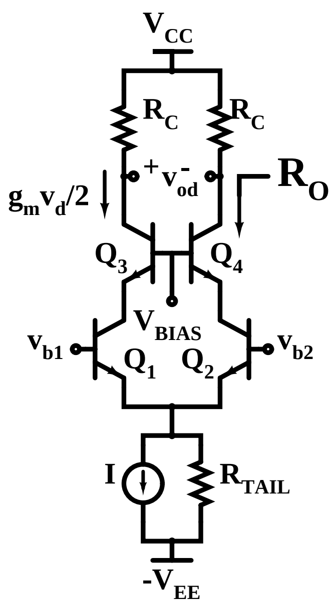


$$i_{OUT} = g_m v_d$$

$$v_{OUT} = i_{OUT} R_O$$

$$R_O = R_{LOAD} || r_{O2} || r_{O4}$$

1

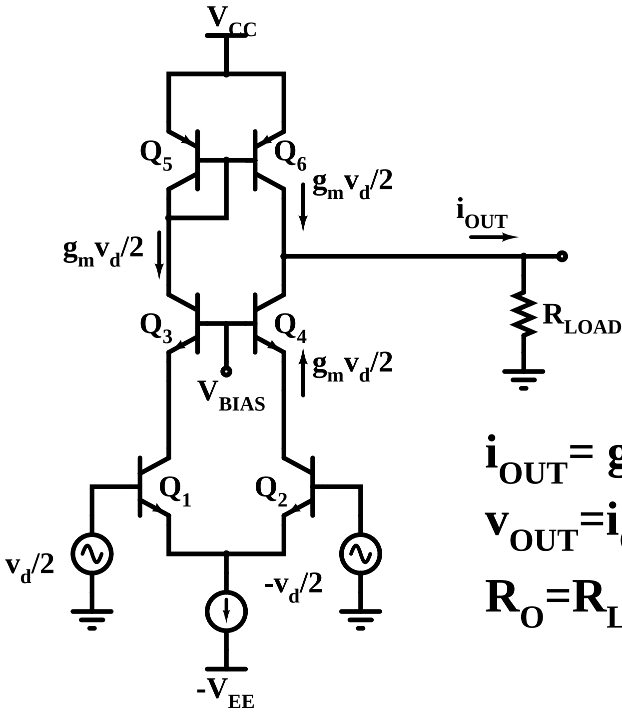


$$R_O = (1 + g_{m4} R_P)\, r_{O4}$$

$$R_P = r_{O2} || r_{\pi 4}$$

$$R_O = (1 + \beta)\, r_{O4}$$

2

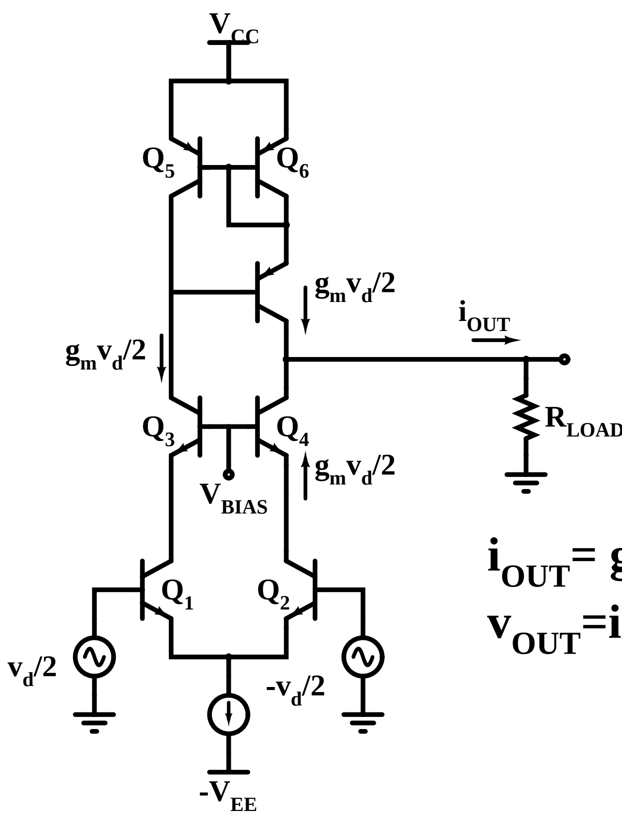


$$i_{OUT} = g_m v_d$$

$$v_{OUT} = i_{OUT} R_O$$

$$R_O = R_{LOAD} || r_{O6} || (1+\beta) r_{O4}$$

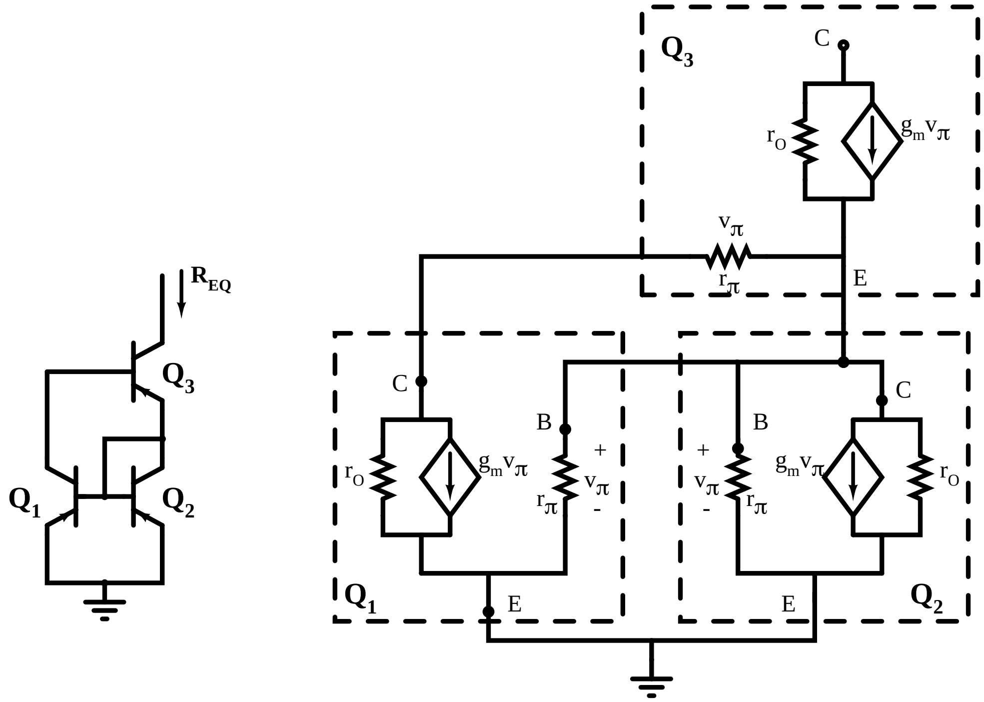
3



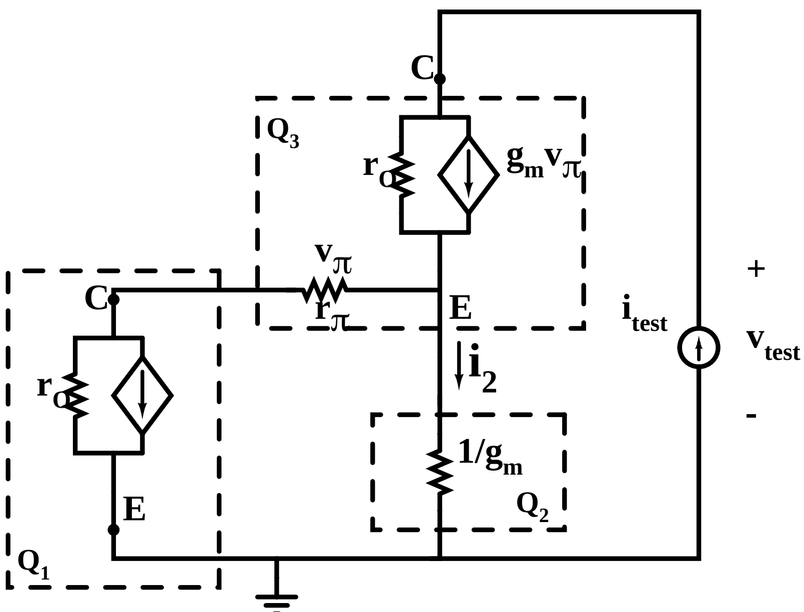
$$i_{OUT} = g_m v_d$$

$$v_{OUT} = i_{OUT} R_O$$

4



5



6

7 Small Signal Analysis of the uA741

These are my class notes for sections 10.3 and 10.4 of Sedra and Smith. They cover the same material than the book, but the approach is a bit different.

The output stage (section 10.5) is only partially included. More complete coverage will be done in the classroom. Nevertheless, observe that since the output stage provides no gain and has a very high input impedance, the voltage gain from differential input to intermediate (second) stage approximates very well the overall amplifier gain.

Sugested practice problems from chapter 10, sections 1 through 4, are: 3, 9, 11, 15, 21, 23, 26, 27, and 31.

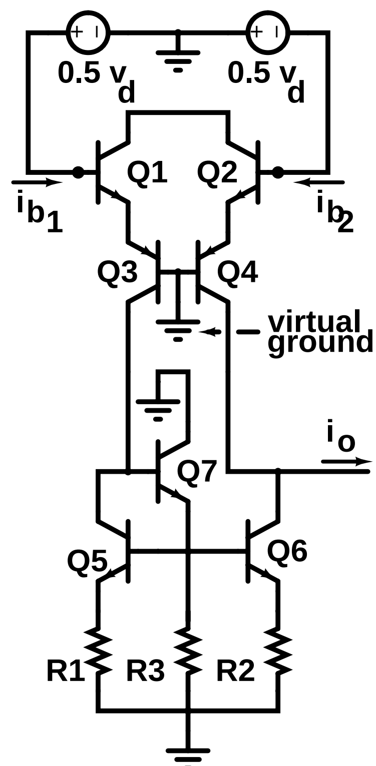
1 Device Parameters

Parameter	npn	pnp
I_S	10^{-14}A	10^{-14}A
β	200	50
V_A	125	50

For Q_{13A} and Q_{13B} assume I_S equal to 0.25×10^{-14}A and 0.75×10^{-14}A, respectively.

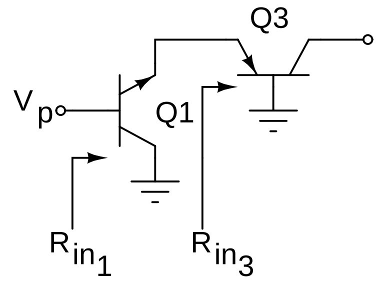
The area of power transistors Q_{14} and Q_{20} is assumed to be three times that of regular transistors.

2 First Stage



2.1 Input Resistance

Because of virtual ground, each differential source sees the following circuit:



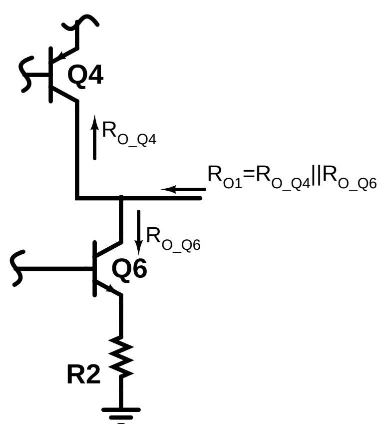
$$R_{in3} = r_{e3} = \frac{V_T}{I_{e3}} = \frac{V_T}{I_{e2}}$$

$$R_{in1} = r_{\pi 1} + (\beta_N + 1)R_{in3} = r_{\pi 1} + (\beta_N + 1)\frac{V_T}{I_{e3}} \approx 2r_{\pi 1}$$

For differential signals: $R_{in} = 4r_{\pi 1}$.

2.2 Output Resistance

$$R_{O1} = R_{O-Q4} \mid \mid R_{O-Q6}$$



For Q6:

$$R_{O-Q6} = r_{O6}(1 + g_{m6}R_2)$$

For Q4:

$$R_{O-Q4} = r_{O4}(1 + g_{m4}R_{eQ4})$$

where R_{eQ4} is the small signal equivalent resistance at the emitter of Q4. Thus

$$R_{eQ4} = r_{e2}$$

and

$$R_{O-Q4} = r_{O4}(1 + g_{m4}r_{e2})$$

Using $I_{C4} = I_{C6} = 9.5\mu A$, we get the following values:

Quantity	Value
$g_{m4} = g_{m6}$	$\frac{I_{C4}}{V_T} = \frac{9.5\mu A}{25mV} = 0.38mA/V$
r_{e2}	$\frac{V_T}{I_{e2}} \approx \frac{25mV}{9.5\mu A} = 2.63k\Omega$
r_{O4}	$\frac{V_{A_{pnp}}}{I_{C4}} = \frac{50V}{9.5\mu A} = 5.26M\Omega$
r_{O6}	$\frac{V_{A_{npn}}}{I_{C6}} = \frac{125V}{9.5\mu A} = 13.16M\Omega$
R_{O-Q4}	$5.26M\Omega\left(1 + 0.38\frac{mA}{V} \times 2.63k\Omega\right) = 10.5M\Omega$
R_{O-Q6}	$13.16M\Omega\left(1 + 0.38\frac{mA}{V} \times 1k\Omega\right) = 18.16M\Omega$
R_{O1}	$10.5M\Omega\,\|\,\|18.16M\Omega = 6.65M\Omega$

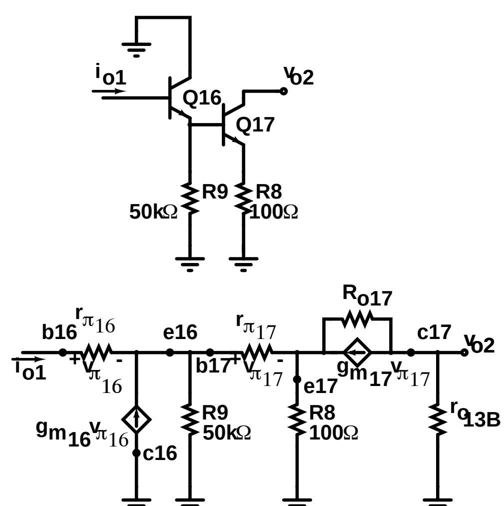
2.3 Transconductance

$$G_{M1} = \frac{i_{O1}}{v_d}$$

Use $i_{O1} = -i_{C6} - i_{C4} = -2i_{e1}$ and $i_{e1} = (\beta_N + 1)\frac{v_d/2}{2r_\pi} = v_d \times \frac{1}{4r_{e1}}$. Thus

$$G_{M1} = -\frac{1}{2r_{e1}} = -\frac{1}{2}g_{m1} = -\frac{1}{2}\frac{9.5\mu A}{25mV} = -0.19\frac{mA}{V}$$

3 Second Stage



3.1 Input Resistance

$$R_{in2} = r_{\pi 16} + (\beta_N + 1) \times (R9\,|\,|\,(r_{\pi 17} + (\beta_N + 1)R_8))$$

Using $I_{C16} = 16.2\mu A$ and $I_{C17} = 550\mu A$, we get $r_{\pi 16} = 200\frac{25mV}{16.2\mu A} = 308.6k\Omega$ and $r_{\pi 17} = 200\frac{25mV}{550\mu A} = 9.09k\Omega$. Thus we get

$$R_{in2} = 308.6k\Omega + 201\,(50k\Omega\,|\,|\,(9.09k\Omega + 201 \times 100\Omega)) = 4M\Omega$$

3.2 Transresistance

$$R_{M2} = \frac{v_{O2}}{i_{i2}} = \frac{v_{O2}}{v_{b16}/R_{in2}} = R_{in2} \times \frac{v_{O2}}{v_{b16}}$$

The output voltage at the collector of Q_{17} depends on the collector resistance. Let this resistance be R_{c17}. Then

$$R_{c17} = r_{o17}(1 + g_{m17}R_8)\,||\,r_{o13B}$$

From $I_{C17} = I_{C13B} = 550\mu A$, $r_{o17} = \frac{V_{Anpn}}{I_{C17}} = \frac{125V}{550\mu A} = 227k\Omega$ and $r_{o13B} = \frac{50V}{550\mu A} = 90.9k\Omega$. Thus

$$R_{c17} = 90.9k\Omega\,||\,227k\Omega \times \left(1 + \frac{550\mu A}{25mV}100\Omega\right) = 80.8k\Omega$$

Using this value, we get

$$\begin{aligned} R_{M2} &= R_{in2} \times \frac{R_{e16}}{r_{e16} + R_{e16}} \times \frac{-g_{m17}R_{c17}}{1 + g_{m17}R_8} \\ &= 4M\Omega \times \frac{18.43k\Omega}{18.43k\Omega + \frac{25mV}{16.2\mu A}} \times \frac{-\frac{550\mu A}{25mV}80.8k\Omega}{1 + \frac{550\mu A}{25mV}100\Omega} \\ &= 4M\Omega \times 0.92 \times -556 = -2044M\Omega \end{aligned}$$

Notice that this can be expressed as a transconductance

$$G_{M2} = \frac{i_{O2}}{v_{i1}} = \frac{-v_{O2} \div R_{c17}}{i_{i1} \times R_{i2}} = \frac{R_{M2}}{R_{i2} \times R_{c17}} = \frac{-2044M\Omega}{4M\Omega \times 80.8k\Omega} = 6.3\frac{mA}{V}$$

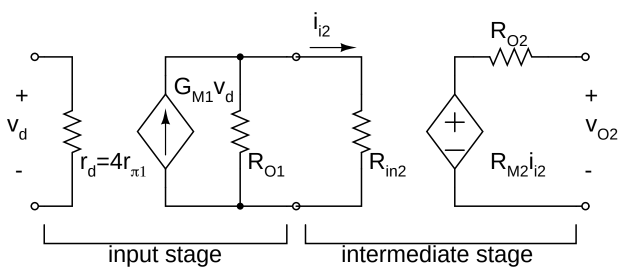
Compare this result with the textbook's of $G_{M2} = 6.5mA/V$ (see page 829).

3.3 Output Resistance

$$R_{o2} = R_{c17} = 80.8k\Omega$$

4 Voltage Gain of Stages One and Two

The voltage gain can be found from the following two-port representation



Using the current divider rule:

$$A_v = \frac{v_{o2}}{v_d} = G_{M1} \times \frac{R_{o1}}{R_{o1} + R_{i2}} \times R_{M2}$$

Using our previous results,

$$A_v = \frac{v_{o2}}{v_d} = -0.19\frac{mA}{V} \times \frac{6.65M\Omega}{6.65M\Omega + 4M\Omega} \times -2044M\Omega = 2.42 \times 10^5$$

5 Output Stage

The output stage, shown in figure 4, consists of a push-pull amplifier. Transistors Q18 and Q19 provide the diode drops necessary for class AB operation.

In analysis, we will replace the Q18/Q19 network by an equivalent resistor, R_{EQ}, whose value we shall now determine. Consider figure 5. A source transformation yields the circuit shown on the right-hand-side sketch. Applying the voltage divider rule to the two resistors on the left gives

$$v_{b_{18}} = v_{\pi_{18}} = \frac{R}{R + \frac{1}{g_{m_{19}}}}$$

where

$$R \equiv R_{10} \parallel r_{\pi_{18}}$$

Applying KCL on the top node yields

$$i_{TEST} = g_{m_{19}} \left(V_{TEST} - v_{\pi_{18}} \right) + g_{m_{18}} v_{\pi_{18}} = g_{m_{19}} V_{TEST} + (g_{m_{18}} - g_{m_{19}}) v_{\pi_{18}}$$

Rearranging

$$\frac{i_{TEST}}{v_{TEST}} = g_{m_{19}} \left(1 + (g_{m_{18}} - g_{m_{19}}) \frac{R}{g_{m_{19}} R + 1} \right) = g_{m_{19}} \frac{1 + g_{m_{18}} R}{g_{m_{19}} R + 1}$$

Thus

$$R_{EQ} = \frac{v_{TEST}}{i_{TEST}} = \frac{1}{g_{m_{19}}} \frac{1 + g_{m_{19}} R}{1 + g_{m_{18}} R}$$

To find the transconductances, we must estimate Q_{18} and Q_{19}'s bias currents. Observe that $v_{BE_{18}} = V_{R_{10}}$. Neglecting the current in the base of Q_{14}, we have that

$$\begin{aligned} I_{13A} &= i_{C_{18}} + i_{C_{19}} \\ i_{C_{18}} &= I_s e^{v_{BE_{18}}/V_T} \\ v_{BE_{18}} &= V_T ln \left(\frac{i_{C_{18}}}{I_s} \right) \\ &= \left(i_{E_{19}} - \frac{i_{C_{18}}}{\beta_N} \right) R_{10} \end{aligned}$$

Thus,

$$R_{10} V_T ln \left(\frac{i_{C_{18}}}{I_s} \right) \approx I_{13A} - i_{C_{18}} - \frac{i_{C_{18}}}{\beta_N}$$

which is one equation in one unknown, $i_{C_{18}}$, and can be solved by sucesive approximations to obtain $i_{C_{18}} = 168\mu A$. From this, we get that $i_{C_{19}} = 15\mu A$, and $R_{EQ} = 165\Omega$.

5.1 Not done yet!

The analysis is not done yet. We still need to calculate the input resistance of the output stage. This is the load of the second stage, and we can combine it with our previous results for the first and second stages to obtain the overall voltage gain of the amplifier. We also need to figure out the the amplifier's output resistance, which is the output resistance of the third stage.

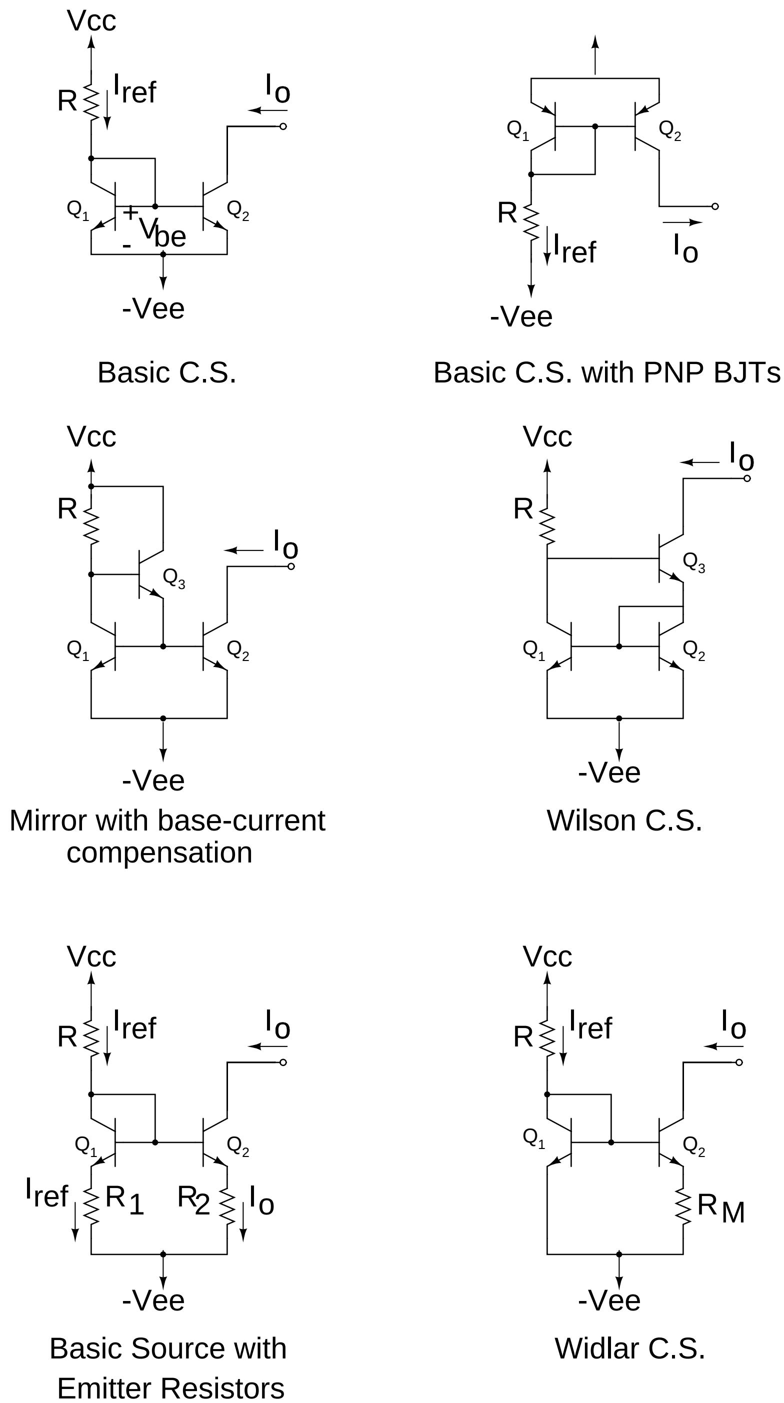


Figure 1: Current sources.

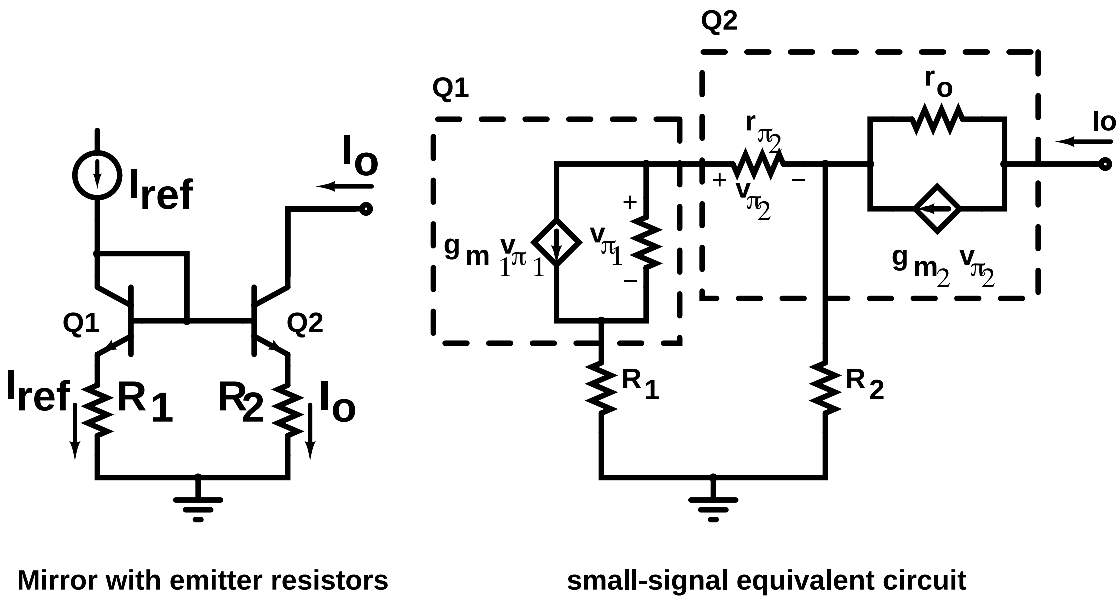


Figure 2: Mirror with emitter resistors and equivalent circuit.

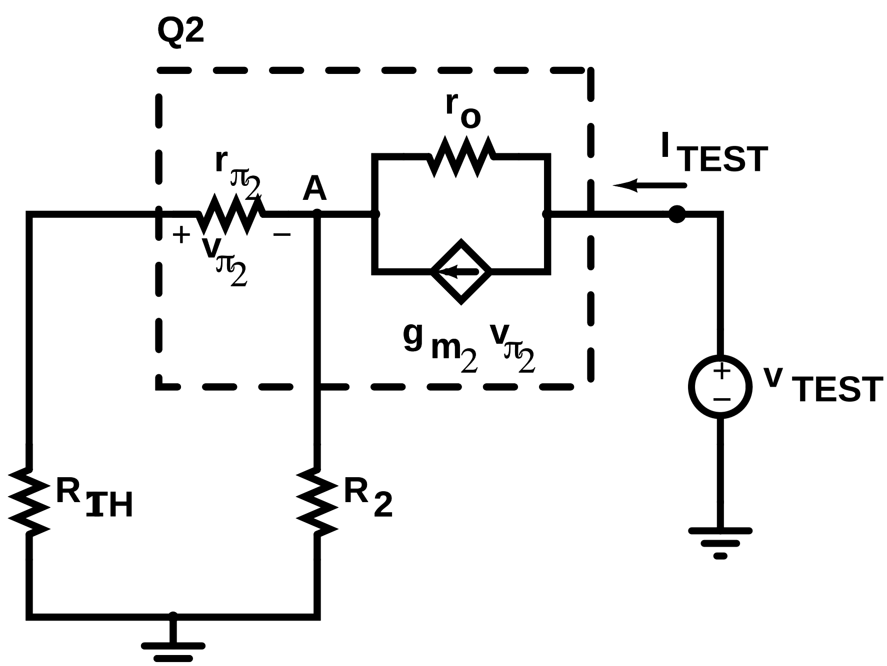


Figure 3: Test circuit with Q1 replaced by R_{TH}.

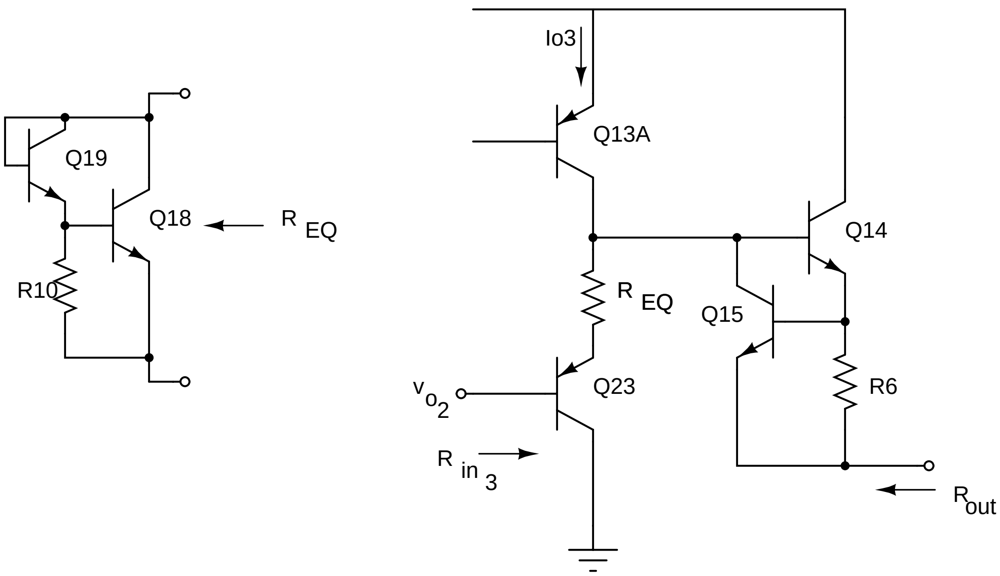


Figure 4: Simplified diagram of the output stage.

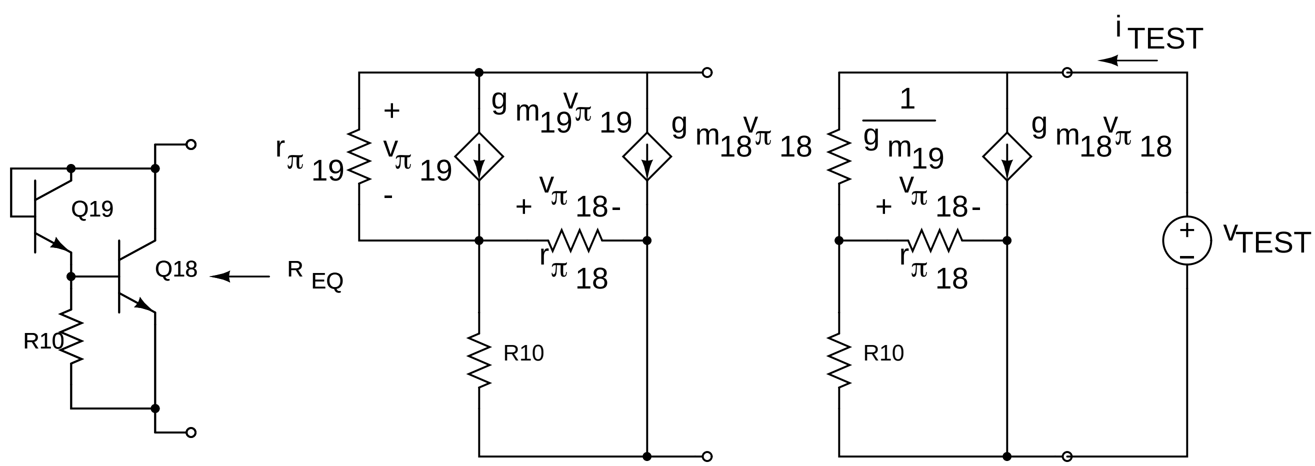


Figure 5: Simplified circuits used to find R_{EQ} (see text).