For electron documents defense there are many special means: document electron-digit signature, post sending and network traffic encryption, various defense system from not sanction access in corporate networks. However only mental user conviction in security of storing, sending and showing of electron documents may to lead to successful system application and stability increase.

The automation of activity of the operator of link is closely connected with the workflow. Complex usage of modern computer technologies of the operator of link will allow providing each participant of the business process with all materials and tools for effective obtaining of necessary documents about operation of the payphones network. One of the major tasks CMPS - automation of business process, at which documents, information and the assignment are transferred (in electronic view) from one participant business process to another for fulfill task according to instruction rules set [2] [4]. For solution of this task the technology Intranet is ideally approaches.

Presence in Microsoft SQL Server the component of integration with the mail system Microsoft Exchange [5] is a good basis for creation of a high-efficiency control system of workflow and office automation oriented to non-failure operation in conditions of the large size of transactions. The application of the similar system will allow to receive significant advantages in cost of preparation and distribution of documents and tasks, in huge saving of time by search and selection of the information, in rise of efficiency and quality of execution of commissions of a leadership, in the support of non-failure operation with the confidential information.

6. CONCLUSION

The document management and works flows processes radically change a workflow application, create environment, where information activity intention and integration will be increase on very high level, providing information fulfill and authentic. In result during working cycle in dozen once reducing watch let to enterprise has been in course of current deal and quickly respond for internal and external environment changing.

In spite of what special tools for necessary environment building is simple in use, complexity of design, innovation and using corporate workflow - applications by previous require professionals in information technology field participating.

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DEPENDABILITY ANALYSIS OF FAULT-TOLERANT MULTIPROCESSOR SYSTEMS BY PROBABILISTIC SIMULATION

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Abstract
The objective of this research is to develop a new approach for evaluating the dependability of fault-tolerant computer systems. Dependability has traditionally been evaluated through combinatorial and Markov modelling. These analytical techniques have several limitations, which can restrict their applicability. Simulation avoids many of the limitations, allowing for more precise representation of system attributes than feasible with analytical modelling. However, the computational demands of simulating a system in detail, at a low abstraction level, currently prohibit evaluation of high-level dependability metrics such as reliability and availability. The new approach abstracts a system at the architectural level, and employs life testing through simulated fault-injection to accurately and efficiently measure dependability. The simulation models needed to implement this approach are derived, in part, from the published results of computer performance studies and low-level fault-injection experiments. The developed probabilistic models of processor, memory and fault-tolerant mechanisms take such properties of real systems, as error propagation, different modes of failures, event dependency and concurrency. They have

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been integrated with workload model and statistic analysis module into a generalised software tool. The effectiveness of such approach was demonstrated through the analysis of several multiprocessor architectures.

**Keywords:** fault-tolerant computer systems, simulation, dependability, probabilistic models.

There are some traditional approaches to provide tolerance to failures and errors. Such fault-tolerant systems incorporate redundancy. The redundancy may consist of a combination of extra hardware and software components, beyond the minimum needed for full system operation. These fault-tolerant systems are often realised as multiprocessors, composed of several processor and memory modules interconnected via hardware mechanisms that manage the redundancy of the system. The hardware mechanisms provide fault-tolerance by detecting, correcting or masking erroneous outputs, and replacing failed modules with spares.

Designing a fault-tolerant computer system is a complex task. The process can be represented by the scheme depicted in Figure 1.

![Diagram of the process of a fault-tolerant computer system design](image)

**Fig 1.** The process of a fault-tolerant computer system design.

Correct methods of estimating dependability measures are required throughout the system design and development process. Once a system realised, its dependability may be empirically determined through life testing. But life testing is usually not feasible for validating fault-tolerant systems, due to their high cost and very high reliability. Analytical models which are commonly represented by combinatorial and Markov modelling, trend to be most useful during early stages of system design. However, analytical models have several limitations, and some methods to more precisely estimate system dependability are required.

Simulation is one of real alternatives to combinatorial and Markov modelling in the advanced stages of system design. The developed approach combines the advantages of the analytical methods and simulation and allows more accurately and efficiently evaluate dependability measures of different levels.

The generalised scheme of simulation model is shown in Figure 2. The model integrates system, workload and fault/error simulation models. Formally, the system model is the set of objects $O$, the set of interconnections $I$, and the set of functions $F$. The set of objects consists of three subsets $P$, $M$ and $FTM$, where $P$ is the set of processor objects, $M$ is the set of memory objects and $FTM$ is the set of fault-tolerance mechanism objects. The set $I$ is a subset of $n$-tupple Cartesian product of $O$. It defines how processors are interconnected to memories through fault-tolerance mechanisms. The value of $n$ depends on a method providing fault-tolerance. Each object $O_m$ is defined by its attribute set $A_m = \{s_m, \pi_m, \tau_m\}$, where $s_m$ - object states, that is attributes defining the system behaviour; $\pi_m$ - some service variables; $\tau_m$ - values equal to a time interval to a next object event $e_m$ on the assumption of other events do not disturb. Events result in changing attributes of some objects. The model trajectory is defined by the sequence $(t_1, e_{m1}), (t_2, e_{m2}), \ldots$ and values of $(s_m, \pi_m, \tau_m)^i$.

![Diagram of the probabilistic simulation model](image)

**Fig. 2.** The components of the probabilistic simulation model.

The operation of fault-tolerance mechanisms, processor and memory modules is governed by corresponding probabilistic models. Most of analytical techniques abstract system at the highest level as a collection of black boxes, for which no detail other than operational or failed status is represented. The developed probabilistic models take on basic information flows within the system is modelled.

The probabilistic models allow to simulate both permanent and transient faults into the processors, memories and fault-tolerance mechanisms of a system. Faults are assumed to occur independently within each component. Their inter-arrival times are randomly sampled from one of standard distributions.

The state of a processor determines what values are driven onto its address and data buses during memory accesses. Processor state changes when it experiences a fault or an erroneous value is read from memory.
(through the fault-tolerance mechanisms). The state of a memory is defined by the contents of its bit-array. The functionality of its addressing-logic is simulated on every memory access. Memory state changes when it experiences a fault or an erroneous value is written into it by the processor (through the fault-tolerance mechanisms). Besides, the probabilistic models take into account such effect as fault latency and propagation.

The workload model is assumed for instruction cycles are continually performed within the modelled system. Behaviour of the application workload is specified by the mean instruction execution rate, the mean rates at which main memory is read and written per instruction, and a locality-of-reference model. The locality-of-reference model determines which memory locations are accessed during an instruction cycle. There workload model implements two models. The first one based on Zipf distributions and were observed for many commercial applications. The second model is corresponded to control systems, where a set of applications is performed periodically.

An instruction is assumed to be successfully executed if no faults are active in the processor and no errors are read from memory during the instruction and data fetches. No errors will be written into memory when an instruction is successfully executed. If a fault is active in the processor or an error is read from memory, the instruction will not execute successfully, and any write into memory that takes place will be erroneous.

The probabilistic models integrated with workload model and statistic analysis module into a generalised software tool. A simulation run has such parameters defined by researcher as the number of processors and memory modules, the number, functionality and interconnection of fault-tolerance mechanisms, the type of fault and repair distributions and its parameters. The effectiveness of such approach was validated through the analysis of several multiprocessor architectures.

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TO A PROBLEM ON COMPONENTS
OPERATION OF A DISTRIBUTED SYSTEM
FOR IMAGE PROCESSING AND ANALYSIS

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Abstract
The modern tasks of processing and analysis of a large scale arrays of the graphics information demand real-time mode and considerable computational resources. The ideology of developing of such systems does not fit to the increasing requirements and does not allow to involve possibilities of these computational resources entirely. In the paper the classifications of such systems and their architectures are conducted. The advantages and disadvantages of existing solutions are detected. The new goals and tasks are posed, the research directions in the field are pointed. The alternative system structure variant for distributed large graphical information arrays processing, the modes of implementation of data exchange processes between separate components of this system, and the ways of its integration with existing information storage and visualization tools are offered. The main component of the tendered system architecture is the intelligent computing core realizing a principle of the expert system. The feature of its operation is encompassed with using of self-learning mode during operation. It allows not only to improve the quality of automatic processing, and to use experience of experts, but also to accumulate its own experience. The possible application areas of such system are considered.

Keywords: image processing and analysis automation, intelligent image analysis, expert systems.

1. INTRODUCTION
The problems of graphic data processing and analysis every year gain the increasing practical value. In 1996 by the governmental order of Russian Federation the information technologies of image recognition and analysis were accepted as "critical" tasks [7]. Today the considerable quantity of software and hardware solutions in this area is built. The motivating factor is the appearance of specialized libraries of signal and image processing (for example, IFLS by Intel corporation) with orientation on a modern microprocessors

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