**EE 5306 Homework**

Resistor Pads

200x200 mils

200 mils space

between all pads

*R*

-Vcc

*R*

Output Match Line

Optimize for L and W

High Impedance Line

W=10 -15 mils, L=/4

Output Match Stub

Optimize for L and W

High Impedance Line

W=10 -15 mils, L=/4

50 mils space

50 line,

L=250 mils

CLY-2

50 mils space

Input Match Line

Optimize for L and W

50 line

L is variable

*R*

Input Match Stub

Optimize for L and W

+Vcc

Low Impedance Line

25 line, L=/4

1 - Consider the amplifier layout above.

1. Identify the bias and matching networks in the circuit.
2. Why is the input and output lines of the amplifier 50?
3. The transistor S parameters are stored in a file designated “CLY2.S2P”. Explain how this information is used by ADS to simulate the performance of the transistor.
4. Explain the purpose of the capacitors at the input and output of the amplifier.
5. Indicate where in the circuit an “MTEE” is required when simulating with ADS
6. How do you think the source lead in the FET is physically connected to ground?

2 - Consider the bias network shown below. It consist of three 4 long lines, two thin lines and an open thick (25 ) line. Using ADS, simulate the performance of this network for fc=1.585 GHz, using a substrate material with r=2.55 and a dielectric thickness of 31 mils. What do you expect to see as input impedance? Plot the input impedance from 1.535 to 1.635 GHz. Is this what you expected? What is the input impedance at dc? Explain. Include plots for S11 in Smith chart format from 1.535 to 1.635 GHz. Hand in your circuit schematic.

High Impedance Line

W=10 -15 mils, L=/4

High Impedance Line

W=10 -15 mils, L=/4

200 mils space

between all pads

Resistor Pads

200x200 mils

Low Impedance Line

25 line, L=/4

*15*

+Vcc

Input

**Note :** Always use the “MTEE” and “MLEF” commands in your simulations.

3 - Consider the Mitsubishi MGF 4301 with Vds=2V and Id=7.5 mA at 12 GHz. Show that the transistor is unconditionally stable at this frequency.



4- Consider the Mitsubishi MGF 4301 with Vds=2V and Id=7.5 mA at 6 GHz. Determine the stability and plot the stability circles if the device is potentially unstable.



5 - Design an amplifier for maximum gain at fc=1.585 GHz using single stub (open) matching sections. The GaAs FET is the Siemens CLY-2 with Vds=6V and Id=150mA. The data can be found at the website (“http://ece.uprm.edu/~colom/cly2.\_6v150mA.s2p”). Use the same substrate material as in problem #2. Use ADS to simulate your amplifier. Do not need to include the bias network in your analysis. Optimize the length and width of the matching network lines if necessary. Keep the input and output match of the amplifier below -10 dB for a 100 MHz bandwidth. Plot the four S-parameters in log/mag format from 1.535 to 1.635 GHz. Hand in your plots and the circuit schematic.

**Note :** Always use the “MTEE” and “MLEF” commands in your simulations.