Universidad de Puerto Rico – Mayaguez
Department of Electrical and Computer Engineering

INEL 4206 – Microprocessors
Final Exam – Summary of Topics

- Material covered by exams I to III (about 50% of the final exam)
- Problem Set 4 – Easy I Simulator
    - Be prepared to make simple modifications to the Easy I simulator like new instructions or new addressing modes
- Basics of Intel 80x86/Pentium Architecture
    - Register Set (16-bit vs 32-bit)
    - Flags (Condition Codes register)
    - Addressing Modes
    - Basics of Instruction Set: Data Movement, Jumps, Arithmetic
    - Should be able to understand the program examples distributed in photocopies.
- I/O Structures
    - Memory-mapped I/O
    - The MIPS/SPIM I/O Architecture
        - Cause and Status Registers
        - Coprocessor 0 instructions: mfc0, mtc0, lwc0, swc0
        - RFE instruction. Returning to interrupted code
        - The keyboard and Display Devices in SPIM
        - User versus kernel mode
    - DMA vs. IO Processors
        - What characteristics set them apart.
        - Advantages and disadvantages of each approach
- Readings:
    - Chapter 8 and Appendix A of Patterson and Hennessy.
    - Lecture 8 transparencies
    - Intel Pentium Architecture slides

REMINDER
FINAL EXAM will be held on Friday May 16, 2003 9:45AM C-317