INEL 4206 Spring 2002 Exámen I 9/21/02

Nombre: _____ **Sección:** _____

¡Anota tu nombre y número de sección en <u>todas las hojas</u> del examen AHORA! (penalidad de 5 puntos)

Tienes 2 horas para completar tres problemas. Lee cuidadosamente todo el examen antes de empezar a trabajar. Muestra todo el trabajo conducente a tu contestación. Podrás recibir crédito parcial por contestaciones parciales siempre y cuando muestres tu trabajo por escrito. Usa tu tiempo inteligentemente. Exito!

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1	45
2	45
3	10
Total	100

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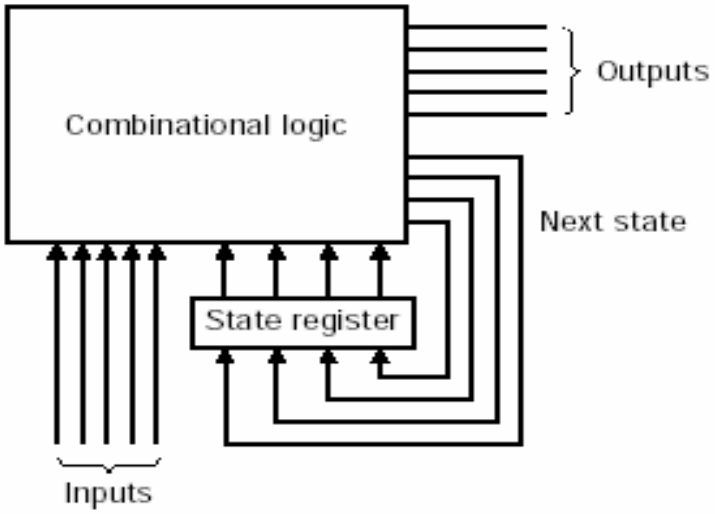
Problema 1. (45 puntos) Finite State Machines

As studied in class, any finite state machines can be implementing as depicted in the following diagram:

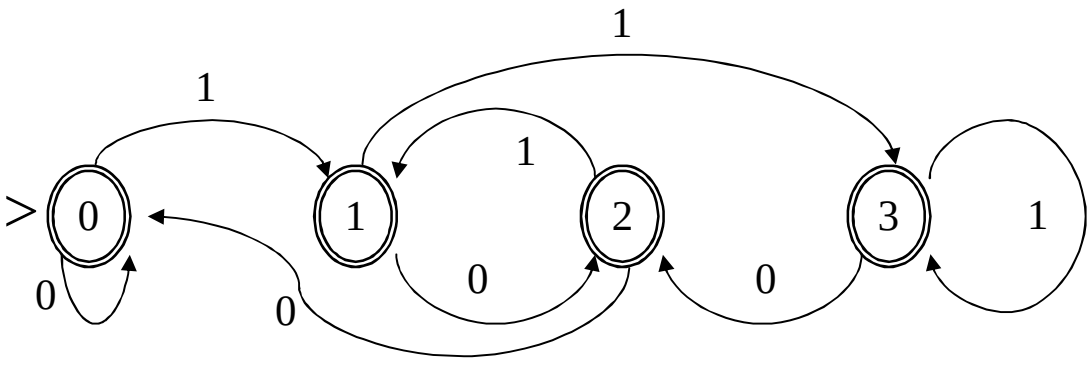


The combinational logic component could be implementing using logic gates or more structured components like multiplexers, ROM's o PLA's.

Consider the following finite state machine that computes the remainder modulo 4 of the number represented by a sequence of bits. For instance, suppose that the machine receives the sequence 101001 representing the number 41 in binary. The machine gets higher order bits first. The machine should end up in state 1, since the remainder of the division of 41 by 4 is 1. For this input, the sequence of states traversed by the machines is:

0 ? 1 ? 2 ? 1 ? 2 ? 0 ? 1

That is, the machine's state number represents the remainder modulo 4 of the number represented by the binary sequence of bits received so far.



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(a) **(5 points)** Write the sequence of states traversed by the machine for the input sequence 10101011.

(b) **(5 points)** Show that the machine operates correctly for this sequence. Convert the binary sequence to its decimal representation and compute its remainder modulo 4.

(c) **(5 points)** Determine the number of flip-flops necessary to implement a sequential circuit implementing the above FSM.

(d) **(15 points)** Provide the state transition diagram for the sequential circuit

Current State	Inputs	Next State

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(e) **(15 points)** Suppose that you want to implement the sequential circuit using the generic diagram mentioned at the beginning of this problem. Moreover, you want to implement the combinational logic component using a ROM. Show the contents of the ROM implementation of the combinational logic component. You must show the address of each ROM word as well as its contents.

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Problema 2. (45 points) Microprocessor Implementation

In this exercise, you will extend the instruction set of the Easy I processor discussed in class (refer to Appendix A for information about the Easy I) with a new instruction Dec describe in the following table:

Symbolic Name	Assembler Example	Action
Dec	Dec	AC - 1 ? AC

a) **(15 points)** WITHOUT MODIFYING THE ALU, show any changes to the Easy 1 datapaths necessary to implement the Dec instruction. Show all you changes on the diagram in the next page. HINT: Consider adding choices for ALU input A. Provide a brief textual description of your proposed modifications in the box below:

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Easy I Datapaths

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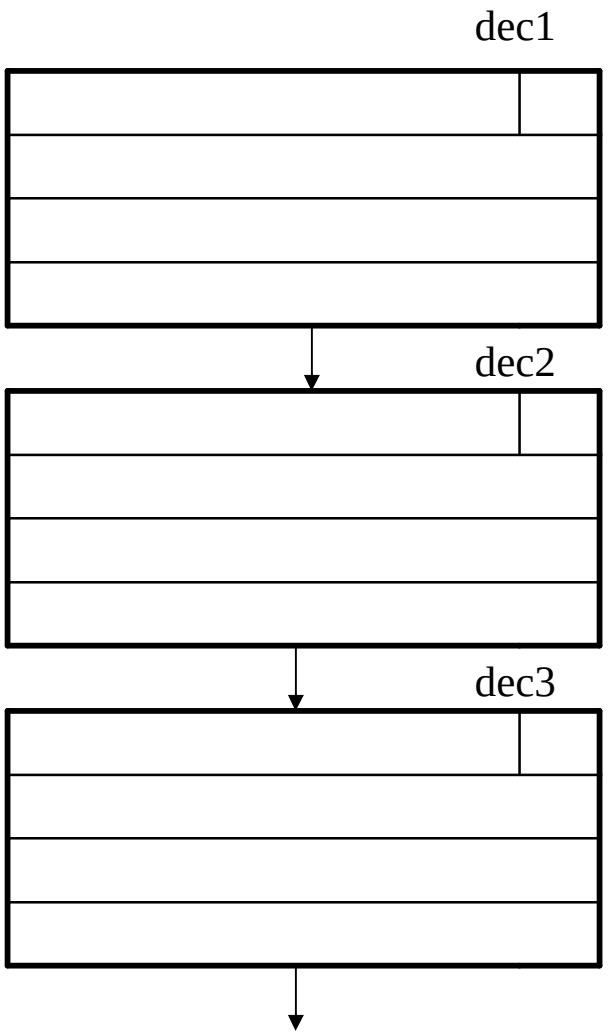
b) **(15 points)** Show a level 2 flowchart implementing the Dec instruction. We provide enough room for your flowchart below, but you may not need all the states depicted below.



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c) **(15 points)** Show any modifications to the Easy I state transition table described in class. Show your changes on the table in the following page. Also, provide a brief textal description of your changes in the box below.

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Easy I State Transition Table

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Problema 3 (10 points) Evaluación del curso

1) Menciona los tres aspectos que mas te gustan de la clase INEL 4206

a)

b)

c)

2) Menciona los tres aspectos que menos te gustan de la clase INEL 4206

a)

b)

c)

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Appendix A. The Easy I processor