Universidad de Puerto Rico
Recinto Universitario de Mayagüez

INEL 4206 – Microprocesadores
Primavera 2002

Ejercicios de práctica
Examen Parcial I

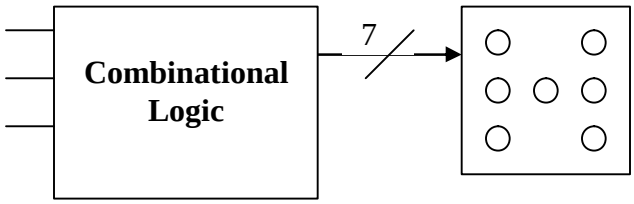
1. **Processor Implementation**. Add an instruction BrL (Branch and link) to the Easy I processor designed in class. You must provide any necessary additions/modifications to the Easy I datapaths, flowcharts and state transition table. The intruction has the following functionality:

Symbolic Name	Assembler Example	Action
BrL	BrL sort	MEM[X-2] <- PC+2 PC <- X

2. **Processor Implementation**. Add an instruction RtL (Return using link) to the Easy I processor designed in class. You must provide any necessary additions/modifications to the Easy I datapaths, flowcharts and state transition table. The intruction has the following functionality:

Symbolic Name	Operands	Action
BrL	RtL sort	PC <- MEM[X-2]

3. **Combinational Logic**. Provide two alternative designs for a combinational circuit to control a Dice LED display. The display has one input for each of 7 LED lights. The combinational circuit must map three inputs encoding a binary representation of a number between 0 and 6 into the 7 control signals controlling the LED's. Design one should use traditional K-Map techniques and should be based on logic gates. The second design should use a ROM or PLA.



4. **Sequential Circuits**. Develop a 3-bit binary cyclic counter using D-Flip-Flops and connect it to the dice display developed in exercise 3 in order to make the display count as follows: 0,1, 2, 3, 4, 5, 6, 0, 1, 2, ...