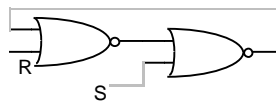


Chapter #6: Sequential Logic Design

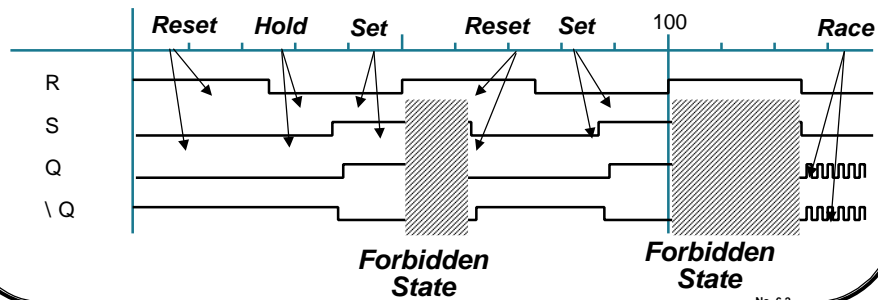
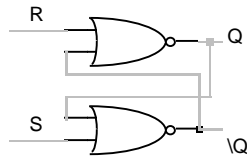
Contemporary Logic Design

No. 6-1

Cross-Coupled NOR Gates

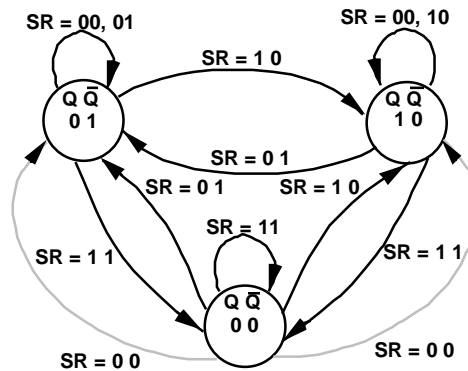


Just like cascaded inverters, with capability to force output to 0 (reset) or 1 (set)



No. 6-2

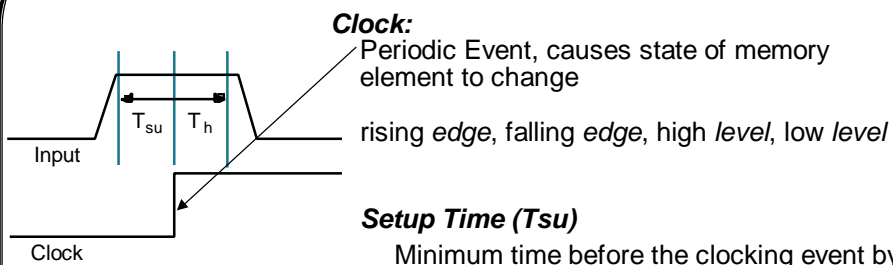
Observed R-S Latch Behavior



Very difficult to observe R-S Latch in the 1-1 state
 Ambiguously returns to state 0-1 or 1-0
 A so-called "race condition"

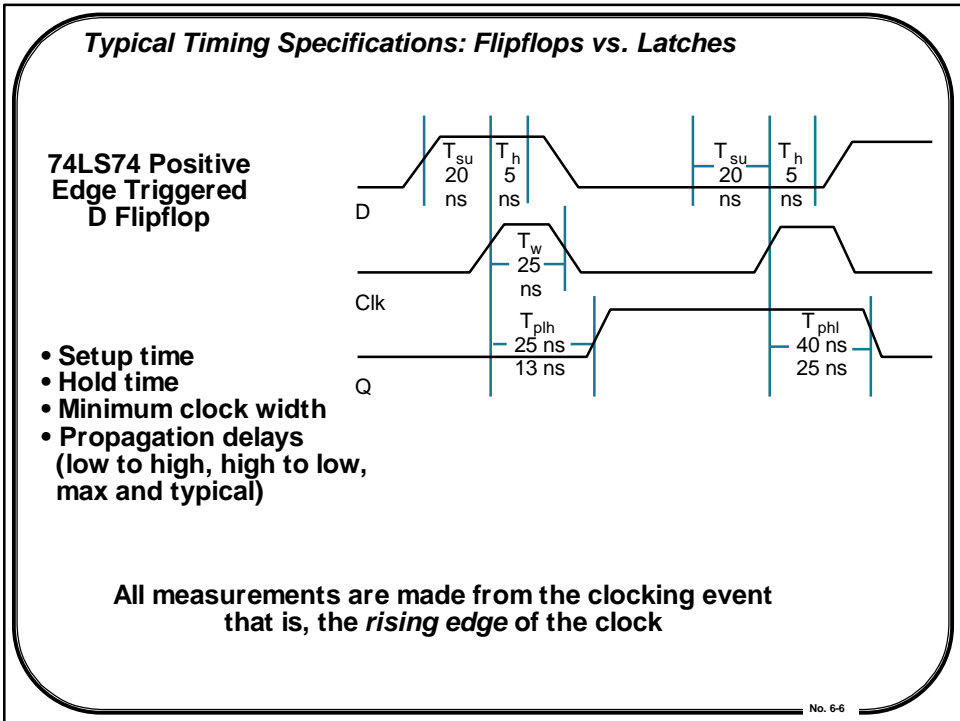
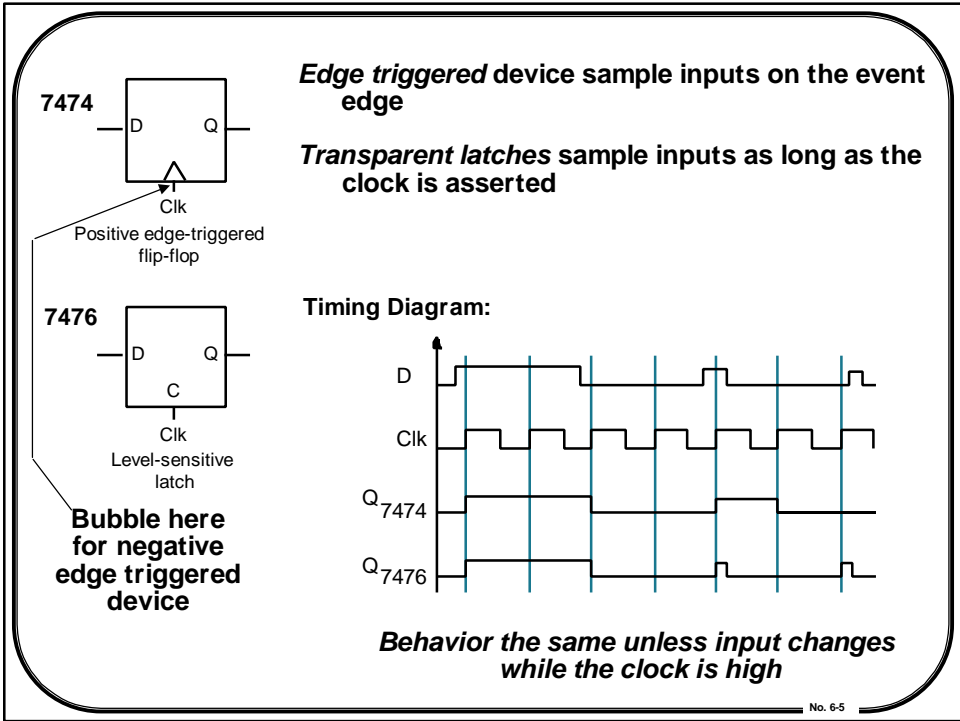
No. 6-3

Definition of Terms



There is a timing "window" around the clocking event during which the input must remain stable and unchanged in order to be recognized

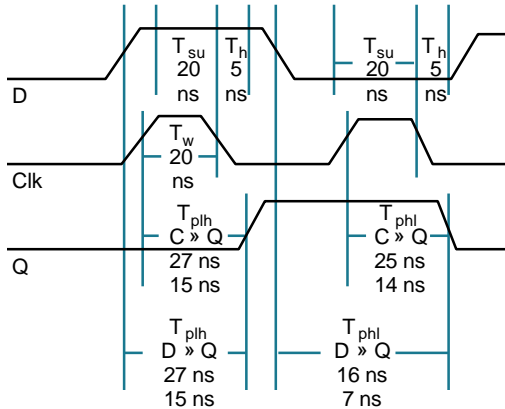
No. 6-4



Typical Timing Specifications: Flipflops vs. Latches

74LS76 Transparent Latch

- Setup time
- Hold time
- Minimum Clock Width
- Propagation Delays:
high to low, low to high,
maximum, typical
clock to output



Measurements from falling clock edge
or rising or falling data edge

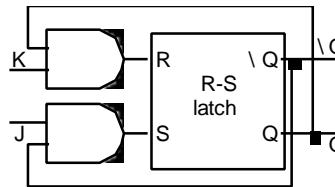
No. 6-7

J-K Flipflop

How to eliminate the forbidden state?

Idea: use output feedback to
guarantee that R and S are
never both one

J, K both one yields toggle



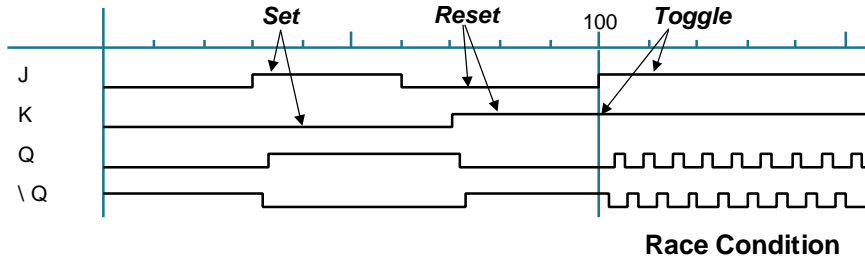
J(t)	K(t)	Q(t)	Q(t+Δt)	
0	0	0	0	HOLD
0	0	1	1	
0	1	0	0	RESET
0	1	1	0	
1	0	0	1	SET
1	0	1	1	
1	1	0	1	TOGGLE
1	1	1	0	

Characteristic Equation:

$$Q+ = Q \bar{K} + \bar{Q} J$$

No. 6-8

J-K Latch: Race Condition

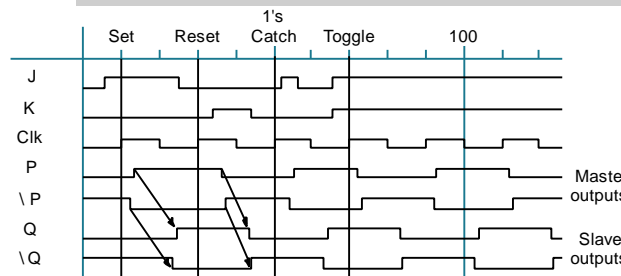
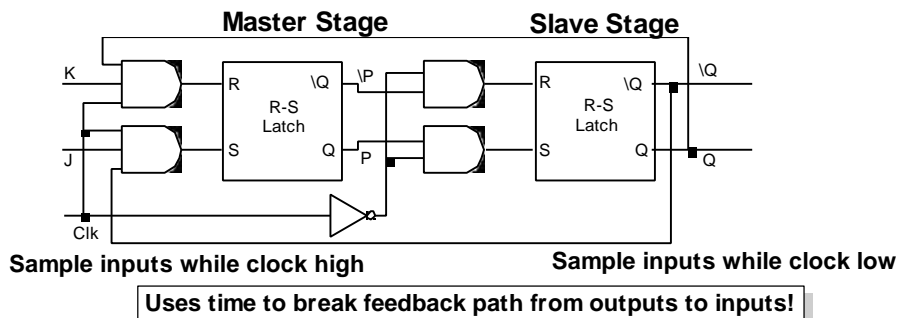


Toggle Correctness: Single State change per clocking event

Solution: Master/Slave Flipflop

No. 6-9

Master/Slave J-K Flipflop



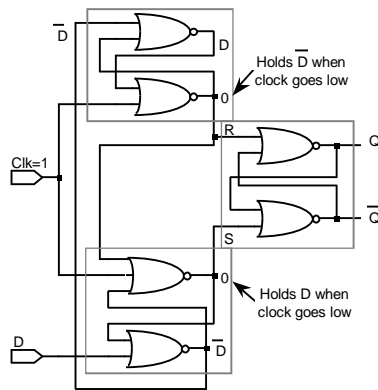
Correct Toggle Operation

No. 6-10

Edge-Triggered Flipflops

1's Catching: a 0-1-0 glitch on the J or K inputs leads to a state change!
forces designer to use hazard-free logic

Solution: edge-triggered logic



Negative Edge-Triggered D flipflop

4-5 gate delays

setup, hold times
necessary to successfully
latch the input

Characteristic Equation:

$$Q^+ = D$$

Negative edge-triggered FF
when clock is high

No. 6-11

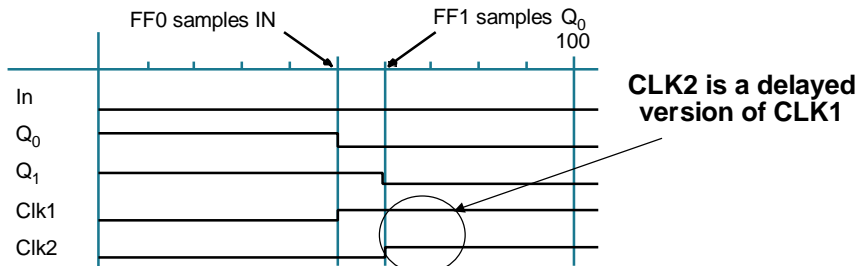
The Problem of Clock Skew

Correct behavior assumes next state of all storage elements determined by all storage elements *at the same time*

Not possible in real systems!

- logical clock driven from more than one physical circuit with timing behavior
- different wire delay to different points in the circuit

Effect of Skew on Cascaded Flipflops:



Original State: $Q_0 = 1, Q_1 = 1, In = 0$

Because of skew, next state becomes: $Q_0 = 0, Q_1 = 0$,
not $Q_0 = 0, Q_1 = 1$

No. 6-12

Realizing Circuits with Different Kinds of Flipflops

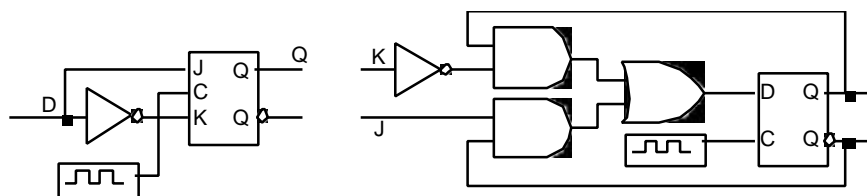
R-S: $Q+ = S + \bar{R} Q$

D: $Q+ = D$

J-K: $Q+ = J \bar{Q} + \bar{K} Q$

T: $Q+ = T \bar{Q} + \bar{T} Q$

Implementing One FF in Terms of Another



D implemented with J-K

J-K implemented with D

No. 6-13

Excitation Tables: What are the necessary inputs to cause a particular kind of change in state?

Q	Q ⁺	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Implementing D FF with a J-K FF:

- 1) Start with K-map of $Q+ = f(D, Q)$
- 2) Create K-maps for J and K with same inputs (D, Q)
- 3) Fill in K-maps with appropriate values for J and K to cause the same state changes as in the original K-map

	D	
	0	1
Q	0	1
1	0	1

$Q+ = D$

E.g., D = Q = 0, Q⁺ = 0
then J = 0, K = X

	D	
	0	1
Q	0	1
1	X	X

J = D

	D	
	0	1
Q	0	1
1	1	0

K = \bar{D}

No. 6-14

Implementing J-K FF with a D FF:

1) K-Map of $Q^+ = F(J, K, Q)$

2,3) Revised K-map using D's excitation table
its the same! that is why design procedure with D FF is simple!

JK Q	J			
	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$Q^+ = D = J\bar{Q} + \bar{K}Q$$

Resulting equation is the combinational logic input to D to cause same behavior as J-K FF. Of course it is identical to the characteristic equation for a J-K FF.