

# Behavioral Modeling of $\Sigma\Delta$ Modulators Based on Symbolic Admittance Matrix

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## Abstract

*This paper proposes a symbolic node admittance matrix representation approach to the behavioral modeling of  $\Sigma\Delta$  Modulators. This new model provides a better representation of the node voltage evolutions without the need for a fixed time step in the system. The newly proposed model provides a more reliable behavioral model of the degrading effects of settling errors and the effects of finite switch resistance. A model based on this approach was build and simulation results are presented. A comparative example of a multibit  $\Sigma\Delta$  Modulator is shown, the signal to noise plus distortion ratio is the measurement of choice for model characterization.*

## 1. Introduction

$\Sigma\Delta$  modulators ( $\Sigma\Delta$ M) are the top choice analog-to-digital (ADC) converters for high resolution large bandwidth applications. Mainstream  $\Sigma\Delta$ Ms are based on SC integrators and other SC techniques.  $\Sigma\Delta$ M are widely used in telecommunications and other portable technologies where the need for low-power, high-resolution, and small size are of critical importance.

$\Sigma\Delta$  simulation in a circuit simulator such as SPICE may take days for a single case. The results from such simulations may be limited by rounding and truncation errors which accumulate through the possibly millions of time steps required for accurate simulation.

Many simulation approaches exist for evaluating  $\Sigma\Delta$ M performance. Simulation approaches based on ordinary differential equations (ODE) are the most commonly used due to the easy to write code and the fast simulation speed [17]. Another simulation approach is the implementation of behavioral models for sub-circuits of the system such as op-amps [13]. Look-up table methodologies have also been implemented. This approach has the lowest simulation time of all other methods [1].

A SC integrator simulation technique with insight to device characteristic variations and viable simulation speed is

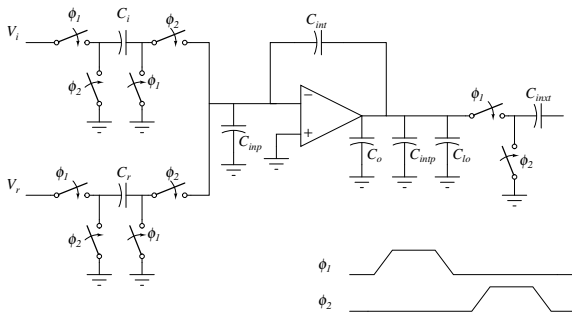
presented. This new technique is based on a symbolic node admittance matrix representation of the system that includes device characteristics and other nonidealities. In section 2 the main consideration for  $\Sigma\Delta$ M degradation are discussed. Section 3 classifies some previous methods of behavioral modeling of  $\Sigma\Delta$ M. In section 4 the proposed model approach is discussed. Section 5 gives some preliminary simulation results. And finally in Section 6 conclusion about the new model are given.

## 2. SC Integrators Considerations in $\Sigma\Delta$ M Modeling

One of the main concerns in  $\Sigma\Delta$ M performance degradation is the integrator incomplete settling [18],[4],[10]. The incomplete settling of integrators becomes one of the most influential parameters limiting the performance of  $\Sigma\Delta$ M when switched capacitor (SC) techniques are implemented. Figure 1 shows a stray insensitive indirect-path SC integrator schematic. Although a complete settling of the integrator is not strictly necessary for  $\Sigma\Delta$ M modeling a strict model becomes crucial in high frequency applications [12]. The need for such a model arises from the relationship between the degrading effects of harmonic distortion and their power consumption [12]. Two parameters characterize the integrator dynamic performance: the gain-bandwidth and the slew rate of the amplifier. Another limiting factor in elaborate  $\Sigma\Delta$ M models is the effect of the non-zero resistance of the sampling switches in the SC integrator [15], [14], [3], [6], [9]. Adding this resistance to the model influences the gain and pole errors. This is due to the fact that the charge transfer is now also determined by the RC time constant of the sampling networks.

## 3. Previous Models

Previous SC integrator models have included the amplifier finite gain-bandwidth (GBW) and slew rate (SR) limitations. However, many of these models take into account the effect of these parameters solely on the integra-



**Figure 1. Stray insensitive indirect-path SC integrator**

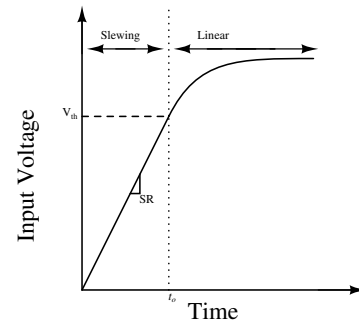
tion phase [18], [16], [2]. Other models also include the degrading effects of harmonic distortion on the sampling phase [11],[13]. The more complete models [13] include both phase for a fixed OTA and SC integrator topology lacking flexibility.

Previously proposed models have established that the transient response of a SC integrator can be divided into three possible scenarios. These include:

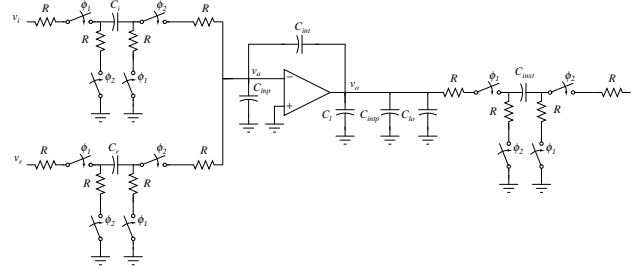
1. Linear evolution: when the amplifier input node voltage is lower than or equal to the amplifier SR.
2. Partial Slew: when the amplifier input node voltage is greater than the amplifier SR. The input node will increase following a constant slope according to the amplifier SR until it reaches a point in time ( $t_o$ ). Time  $t_o$  is reached when the input node voltage is equal to the amplifier SR. From this point forward the input node will evolve exponentially.
3. Slew: when a partial slew evolution is unable to reach time  $t_o$ .

The previous discussion shows that variables SR and  $t_o$  determine the integrator evolution model. Fig. 2 shows an illustrative example of the input voltage of a partial slew amplifier.

This approach has been found to overestimate the settling error of the integrator [5]. Many of these approaches are based on assumption that, although holding for nominal cases, they introduce significant errors under worst case scenarios. As an example, the most common models ignore the relationship between the  $g_m$  and  $g_o$  of the OTA. This holds true for  $g_m \gg g_o$  but as  $g_m$  decreases the minimum power needed for a desired resolution under this assumption has been found to be overestimated for as much as 40%[7]. This approach also assumes an abrupt jump of the node voltages as the switches open and close. This approximation has been shown to overestimate the voltage drop



**Figure 2. Transient response of a partial slew amplifier.**

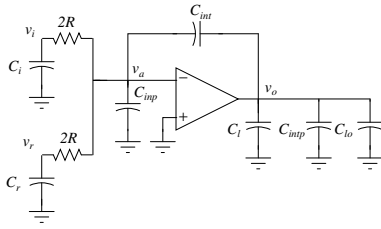


**Figure 3. SC integrator model including the finite switch resistance.**

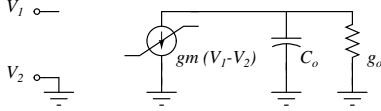
due to the redistribution of the capacitor charges [7]. The final missing influential assumption is the neglect of finite switch resistances. This approximation is used due to an increase in the number of nodes in the integrator model as we include these resistances. An increase in the number of nodes implies a significant increase in the complexity of the equations. Fig. 3 shows a SC integrator model including the finite switch resistances.

#### 4. The Symbolic Node Admittance Matrix Model

This new approach to the behavioral modeling of a SC integrator is based on the symbolic representation of the system node admittance matrix. It takes advantage of developments in speed of symbolic mathematical software. The symbolic representation of a system node matrix of a linear integrator such as the one shown in Fig. 4 during the integration phase with lumped resistance parameter can be written as given in Equations 1, 2.



**Figure 4. SC integrator including the finite switch resistance during the integration phase with lumped resistance parameter.**



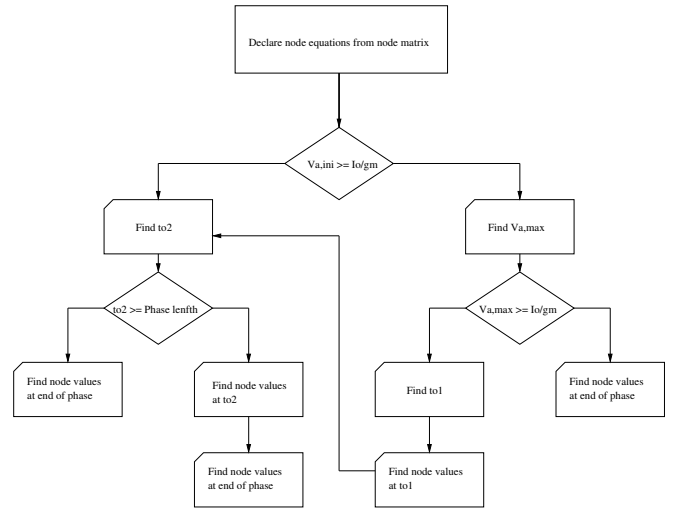
**Figure 5. OTA model including the output admittance.**

$$G = \begin{bmatrix} sC_i + \frac{1}{2R} & 0 & \frac{-1}{2R} & 0 \\ 0 & sC_i + \frac{1}{2R} & \frac{-1}{2R} & 0 \\ \frac{1}{2R} & \frac{1}{2R} & \frac{-1}{R} - s(C_{int} + C_{inp}) & sC_{int} \\ 0 & 0 & sC_{int} - g_m & g_o - sC_x \end{bmatrix} \quad (1)$$

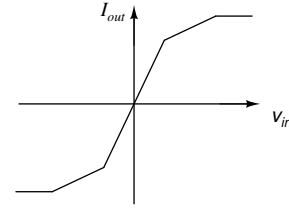
$$V = \begin{bmatrix} C_i V_i(0) \\ C_r V_r(0) \\ -(C_{int} + C_{inp}) V_a(0) + C_{int} V_o \\ -V_o C_x + V_a C_{int} \end{bmatrix} \quad (2)$$

In this model,  $C_x = C_{int} + C_{inp} + C_o$ ,  $V_a$ ,  $V_o$ ,  $V_i$ , and  $V_r$  are the respective node voltage of Fig. 4. The OTA model used for this derivation is shown in Fig. 5. The slewing integrator can be described in the same manner for both sampling and integration phase.

From the above system we can use a symbolic software package such as Maple or Mathematica to determine the node voltages equations in terms of the Laplace operator. These equations are determined for a VCCS and an independent current source for the OTA model. These two set of equations model the possible OTA states, linear and saturation. We use these equations to determine the inverse Laplace function as to determine the transient node equations. This process is automated and no need for hand calculation is needed. These equations are then used as inputs to the flowchart in Fig. 6. The proposed method is considers of the finite switch resistance of the system and automates of the node equations development. The simplicity and flexibility of the proposed approach allows for further improvements. Future models may include an OTA model with a multiple linear regions. This new linear regions would al-



**Figure 6. Flowchart of proposed behavioral model**



**Figure 7. Piece-wise linear OTA transfer function.**

low to better model the linear to slew transition of the system. Fig. 7 shows an illustrative example of piece-wise linear OTA function. Another improvement might be a two stage OTA [8].

The first step in the model algorithm is to determine whether the starting input voltage  $V_a$  requires that the limited VCCS inside the OTA model operates in the linear or non-linear region. This is equivalent to determining whether or not the integrator is slewing. The threshold voltage between these two regions ( $V_{th}$ ) is said to be  $I_{max}/g_m$ . After this comparison is stated we establish which set of equations, slewing or linear OTA, is to be used in the following steps.

If the OTA was said to be slewing then we must find the time ( $t_{o2}$ ) at which it stops slewing. This is the left side of the flowchart in Fig. 6. Determining whether or not the voltage of the node is below  $V_{th}$  at the end of the present phase suffices for the determination of the existence of  $t_{o2}$ . If  $t_{o2}$  is needed a numerical method is applied to determine this point in time.

In a case where  $t_{o2}$  is exists, only the initial conditions

are needed to calculate the final values of the node voltages. If  $t_{o2}$  is found then the system is said to be slewing until  $t_{o2}$ . We must now find the node voltages at this point in time. From this point on we say that the system is linear implying a change in the model equations from slewing to linear model. The final values of the node voltages at time  $t_{o2}$  are used as the initial condition of the linear system. The final node voltages are calculated using these initial condition up to the end of the current phase, this is the difference between  $t_{o2}$  and the length of the current phase.

Now, the case where the system is said to be linear in the beginning is discussed. As before, the system is said to be linear if the initial input voltage  $V_a$  is lower than  $V_{th}$ , this is the right hand side of the flowchart in Fig. 6. The next step is to determine whether at some point in time the system will begin to slew or not. To do so the maximum value of  $V_a$  ( $V_{a,max}$ ) during the current phase is determined.  $V_{max}$  is equivalent to the inflexion point of the  $V_a$  first derivate. If at some point in time  $V_{a,max}$  is greater than  $V_{th}$ , then from this point on the system is said to be slewing. Otherwise the system is said to be linear. If such a point in time is found ( $t_{o1}$ ), the node voltages at  $t_{o1}$  are found and these are used as the initial conditions for the development of a slewing system as before. If  $V_{a,max}$  never reaches the value of  $V_{th}$  then the system is said to be linear all through the current phase and its node voltages are found.

It can be inferred from the above discussion that the number of symbolic node voltage calculations for each phase is drastically reduced to a maximum of four. These symbolic representations of the node voltages are only dependent on initial conditions and time. This allows for the system symbolic representation to be calculated only once for the slewing and linear cases at the beginning of the pseudo code.

The system symbolic representation provides the accuracy needed compared to previous behavioral models. A robust analysis with a small compromise in speed is also accomplished. From the above, a Matlab model has been developed. The Matlab platform was chosen because it provides a symbolic toolbox based on the Maple kernel. Matlab also provides a wide range of DSP functions allowing for information post-processing. This also allows for a fully integrated design analysis tool to be developed on the same software interface.

## 5. Simulation Results

The correctness of the system was proved by a comparison of the model against a SPICE simulation. Since no time step technique is used a graphical representation of the system is impractical. The critical points in the code were compared. These critical points are:  $V_{a,max}$ ,  $t_{o1}$ ,  $t_{o2}$ , and  $V_{a,end}$ ; where  $V_{a,end}$  is the final phase value of the input

node voltage. Tables 1, 2, 3 show the results for the different scenarios. Table 1 lacks the critical points  $t_{o1}$  and  $t_{o2}$  since they are not needed for the system evolution description. The same is observed for  $t_{o2}$  in Table 3.

The speed of the proposed approach was compared to a time step approach [9] inside MatLab. The analysis included a single integration phase for the second scenario (partial slew) for both models. The integration phase was divided into 1,000 steps for the fixed time step as to ensure proper zero-crossing detection. For the proposed approach the maximum number of points needed is four. This is a constant in the approach independent of the desired resolution. The critical points difference between models was below 1%. The proposed model average evaluation time was three seconds meanwhile for the fixed time step the average time was fifteen seconds.

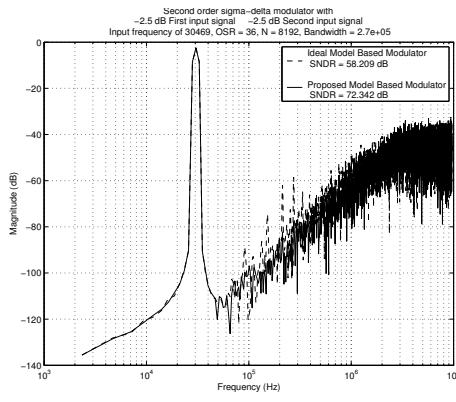
As a comparative example a 3-bit, five-level, second-order  $\Sigma\Delta M$  using the new SC model was simulated and the results compared to those of previous models. Fig. 8 shows some preliminary results. The relevant parameters are: oversampling ratio of 36, and a sampling frequency of 19.2MHz. Thermal and capacitor mismatch noise sources were not included as to isolate the integrator induced distortion. Fig. 8 shows the power spectrum of an ideal system with its nominal slew rate. From the shown simulation it can be seen that ideal models overestimated the signal to noise plus distortion ratio of the modulator. The error is due to the underestimation of the OTA effective slew rate and its dithering effects. Fig. 9 shows a comparison of the power spectrum from a previous model [11] and the proposed model. From the shown results an increase in the system resolution is observed. This increase in resolution is due to the overestimation of the harmonic distortion by the previous model.

## 6. Conclusion

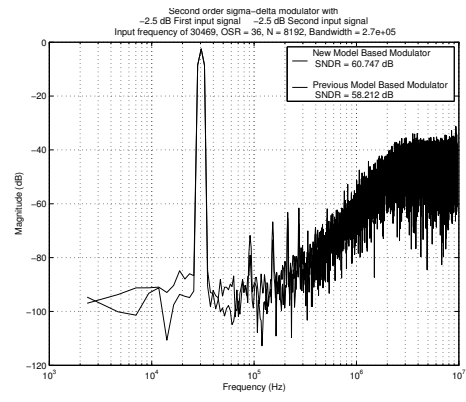
The sigma-delta modulator has been chosen for the last few years as the main resource for high-speed, high-resolution, and low-power data converters. Accurate modeling of essential blocks, such as the SC integrator, is crucial for the design of sigma-delta modulators. Many approaches derive methods for the improvements of behavioral models of such block. In this paper we have presented a symbolic

**Table 1. First scenario input node critical points during integration phase**

|             | SPICE           | New Model       |
|-------------|-----------------|-----------------|
| $V_{a,max}$ | -0.0187 V       | -0.0186 V       |
| $V_{a,end}$ | -41.225 $\mu V$ | -39.991 $\mu V$ |



**Figure 8. Power spectrum of modulator output with nominal values**



**Figure 9. Power spectrum of modulator output. Previous models versus proposed method.**

admittance node matrix approach. This approach provided added accuracy to already studied models that lacked such a feature. A higher SNDR resolution was found when compared with previous models. The OTA SR requirements were found to be more relaxed than what were expected from previous models. A novel behavioral modeling approach is shown with promising preliminary results.

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**Table 2. Second scenario input node critical points during integration phase**

|             | SPICE     | New Model |
|-------------|-----------|-----------|
| $V_{a,max}$ | -0.1990 V | -0.1997 V |
| $V_{a,end}$ | -0.546 mV | -0.399 mV |
| $t_{o1}$    | 5.870 ps  | 5.817 ps  |
| $t_{o2}$    | 5.467 ns  | 5.467 ns  |

**Table 3. Third scenario input node critical points during integration phase**

|             | SPICE     | New Model |
|-------------|-----------|-----------|
| $V_{a,max}$ | -0.8106 V | -0.8107 V |
| $V_{a,end}$ | -0.0487 V | -0.0477 V |
| $t_{o1}$    | 1.340 ps  | 1.335 ps  |

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